QUESTION BANK

Name of the Department : **M.E (VLSI DESIGN) / Electronics And Communication Engineering**

Subject Code & Name : **VL5102 / CAD for VLSI Circuits**

Year & Semester : **I / I**

UNIT: I – INTRODUCTION TO VLSI DESIGN FLOW

PART-A

1. List the three domains present in y chart.

1. Behavioural domain
2. Structural domain
3. Physical domain

2. Define layout editor. (NOV 2010,MAY 2012)

When designing full-custom chips, the designer should have the possibility to modify the layout at the level of mask patterns. The computer tool that supports this action is called layout editor.

3. What are verification methods present in VLSI? (NOV 2009)

1. Prototyping
2. Simulation
3. Formal verification

4. Define clique. (MAY 2010,NOV 2009)

A sub graph that is complete, and that is not contained in a larger complete sub graph, is called a clique.

5. Define selfloop and multi graph.

The degree of a vertex is equal to the number of edges incident with it. An edge (u,u)i.e.one stating and finishing at the same vertex, is called a selfloop. A graph without selfloops but with parallel edges is called a multi graph.

6. What are the computational complexities present in VLSI? (MAY 2011, NOV 2010)

Time complexity: which is a measure for the time necessary to accomplish a computation.

Space complexity: which is a measure for the amount of memory required for a computation.

7. Differentiate BFS and DFS.

One need to traverse the graph in one way or the other and do something with the nodes and/or edges that encounters during the traversal.one way of doing this is by means of depth first search. A breadth first search is an alternative to depth first search for systematically visiting all vertices of a graph.

8. What is a spanning tree? (NOV 2009)

A tree is a connected graph without cycles. A spanning tree of a connected graph G(V,E) is a sub graph of G that is a tree and contains all vertices of V.

9. Differentiate tractable and intractable problems.

A problem that can be solved in a polynomial time is, therefore called tractable and NP-complete. A problem that can be solved in a non-polynomial time is, therefore called intractable and NP-hardness.

10. Define Backtracking. (MAY 2011)

The principle of backtracking for an exhaustive search of the solution space is to start with an initial partial solution in which as many variables as possible are left unspecified, and then to assign values to the unspecified variables until either a single point in the search space is identified or an implicit constraint makes it impossible to process more unspecified variables.

11. Define Branch and bound. (MAY 2008)

The modification of back algorithm that provides in killing partial solutions is called branch and bound.

12. What is dynamic programming?

Dynamic programming is a technique that systematically constructs the optimal solution of some problem instance by defining the optimal solution in terms of optimal solutions of smaller size instances.

13. Define integer linear programming. (NOV 2007)

Integer linear programming (ILP) is a specific way of casting a combinatorial optimization problem in a mathematical format.

14. What is simulated annealing?

Simulated annealing (sometimes called statistical cooling) performs a computation that is analogous to a physical process. In the physical process concerned, a material is first heated up to a temperature that allows all its molecules to move freely around (the materials becomes liquid),and is cooled down very slowly.

15. Define tabu search. (MAY 2008, NOV 2010)

Simulated annealing allows many uphill moves at the beginning of the search and gradually decreases their frequency. In this way, a convergence mechanism is imposed to the search. The tabu search method, on the other hand, does not directly restrict uphill moves throughout the search process.

16. Write the advantages of using genetic algorithm in CAD. (MAY 2010)

As in local search and its related methods, a genetic algorithm also works with fully specified solutions f included in the set of feasible solutions F. The algorithm simultaneously keeps track of a set of feasible solutions.

17. When is Application Specific System processors (ASSPs) used in an CAD?

An ASSP is dedicated to real-time video processing applications such as video conferencing, video compression and decompression systems. It is used as an additional processing unit for running application specific tasks in the place of processing using embedded software.

18. What is the need for LCD and LED displays? (NOV 2011)

Uses of LCD and LED display:

1. It is used for displaying and messaging.
2. Example: Traffic light status indicator, remote controls, signals, etc.,
3. The system must provide necessary circuit and software for the output to LCD controller.

20. Define device driver.

A device driver is software for controlling, reading, sending a byte of stream of bytes from/to the device.

PART – B

1. Describe in detail about gajski's Y chart. (MAY 2010, NOV 2009)
2. Explain in detail about Algorithmic graph theory and computational complexity. (NOV 2010)
3. With a pseudo code, write the data structure representation of graphs.
4. With a pseudo code, write the data structure to repeat the graphs.
5. Describe tractable and intractable problems in detail. (MAY 2011)
6. With an example, explain BFS and DFS algorithm. (MAY 2010)
7. Explain Dijkstra's shortest path algorithm with an example. (NOV 2010)
8. Discuss the general purpose methods for combinatorial optimization. (MAY 2011,NOV 2012)
9. Explain Backtracking and branch and bound in detail.

UNIT: II – LAYOUT , PLACEMENT AND PARTITIONING

PART-A

1. What is layout compaction? (MAY 2011)

At the lowest level, the level of mask patterns for the fabrication of the circuit. A final optimization can be applied to remove redundant space. This optimization is called layout compaction.

2. What are the design rules available for fabrication of IC? (MAY 2009,NOV 2010)

The mask patterns that are used for the fabrication of an integrated circuit have to obey certain restrictions on their shapes and sizes. These restrictions are called the design rules.

3. What are the common types of minimum distance rules? (MAY 2010)

The most common types of minimum distance rules are

1. Minimum width,
2. Minimum separation
3. Minimum overlap

4. What is the use of symbolic layout?

Symbolic layout can normally be created interactively on graphics computer screen, by means of a symbolic layout editor or it can be specified in textual form by means of a formal layout language

5. Write the applications of layout compaction.(NOV 2010,MAY 2009)

1. Converting symbolic layout to geometric layout
2. Removing redundant area from geometric layout
3. Adapting geometric layout to a new technology
4. Correcting small design rule errors

6. Define DAG. (MAY 2012,NOV2013)

A constraint graph derived from only minimum-distance constraints has no cycles .It is called a directed acyclic graph, often denoted by abbreviation DAG.

7. What are the types of placement? (MAY 2013)

1. Constructive placement
2. Iterative placement

8. What do you mean by placement? (MAY 2012,NOV 2010)

The wiring should realize exactly the interconnections specified in the structural description. The determination of the wiring patterns on chip forms routing problem. During placement, it is sufficient to estimate the area occupied by wiring.

9. Define partitioning.

The partitioning deals with splitting a network into two or more parts by cutting connections.

10. What are the common metrics for wire length estimation?

- Half perimeter
- Minimum rectilinear spanning/steiner tree

11. Differentiate constructive placement and iterative placement. (NOV 2012)

Constructive placement: the algorithm is such that once the coordinates of a cells have been fixed they are not modified anymore.

Iterative placement: all cells have already some coordinates and cells are moved around their positions are interchanged etc, in order to get a new configuration

12. Expand a) SPI b) SCI.

SPI - SERIAL PERIPHERAL INTERFACE
SCI - SERIAL COMMUNICATION INTERFACE

13. What are the features of SPI? (NOV 2009)

- SPI has programmable clock rates
- Full-duplex mode
- Crystal clock frequency is 8MHz

14. Define software timer.

A software timer is software that executes the increase/decrease count value on an interrupt from timer or RTC. Software timer is used as virtual timing device.

15. What are the forms of timer?

- Hardware interrupt timer
- Software timer
- User software controlled hardware timer
- RTOS controlled hardware timer
- UP/DOWN count action timer
- One-shot timer (No reload after overflow and finished states)

16. Define RTC (MAY 2012)

RTC Stands for Real Time Systems. Once the system starts, do not stop/reset and the count value cannot be reloaded.

17. What is I2C? (NOV 2007)

Inter- Integrated Circuit (2-wire/line protocol) which offers synchronous communication. Standard speed: 100Kbps and High speed: 400 Kbps

18. What are the four types of data transfer used in USB?

- Controlled transfer
- Bulk transfer

19. Mention some advanced bus standard protocols. (MAY 2003,NOV 2010)

1. GMII (Gigabit Ethernet MAC Interchange Interface)
2. XGMI (10 Gigabit Ethernet MAC Interchange Interface)
3. CSIX-1 6.6 Gbps
4. Rapid IO interconnect specification v1.1 at 8 Gbps

20. What do you meant by high speed device interfaces?

Fail-over clustering would not be practical without some way for the redundant servers to access remote storage devices without taking a large performance hit, as would occur if these devices were simply living on the local network. Two common solutions to this problem are double-ended SCSI and fibre-channel.

21.Mention some I/O standard interfaces.

HSTL - High Speed Transceiver Logic (Used in high speed operations)

SSTL - Stub Series Terminated Logic (Used when the buses are needed to isolate from the large no. of stubs)

PART – B

1. Describe the design rules with brief notes. (MAY 2011)
2. Write short notes on symbolic layout.(NOV 2010,MAY 2009,MAY 2012)
3. Write short notes on
   (i) Problem formulation
   (ii) Time complexity
   (iii)Wire length estimation (MAY 2009, NOV 2011, NOV 2012)

4. Explain In detail about constraint graph compaction.
5. Explain in detail about bellman ford and liao wong algorithm.(MAY 2008,)
6. Explain how placement is done in VLSI Design. (NOV 2011,NOV 2009)
7. Explain how partitioning is done in VLSI Design.
8. Explain in detail about placement and partitioning algorithms in detail. (May 2012,NOV 2013)
9. Explain KL algorithm in detail.

UNIT: III – FLOOR PLNNING AND ROUTING

PART-A

1. Define floor planning. (NOV 2008)

One can estimate the area to be occupied by the various sub blocks and together with a precise or estimated interconnection pattern, try to allocate distinct regions of the integrated circuit to the specific sub blocks. This process is called floor planning.

2. What are leaf and composite cells?

Cells are built from other cells, except for those cells that are at the lowest level of hierarchy. These lowest level cells are called leaf cells. Cells that are made from leaf cells are called composite cells.

3. What are the optimization problems in floor planning? (MAY 2010,NOV 2009)

1. Mapping of a structural description to a floor plan
2. Floor plan sizing
3. Generation of flexible cells

4. Define shape function.

The minimal height given as a function of the width is called the shape function of the cell.

5. Write the sizing algorithm for slicing floor plan. (MAY 2003,MAY 2006)

Construct the shape function of the top level composite cell in a bottom-up fashion starting with lowest level and combining shape functions while moving upwards.

Choose the optimal shape of the top-level cell.

Propagate the consequences of the choice for the optimal shape down the slicing tree until the shapes of all leaf cells are fixed.

6. What is the use of routing? (NOV2006)

The specification routing problem will consist of the position of the terminals, netlist that indicates which terminals should be interconnected and the area available for routing in each layer.

7. What are the types of local routing problems? (MAY 2009)

- The number of wiring layers
- The orientation of wire segments
- Gridded or gridless routing
- Permutability of terminals

8. Mention the steps involved in Area routing. (NOV 2002)

1. Wave propagation
2. Backtracking
3. Clean-up

9. Define channel routing. (NOV 2011,NOV 2005)

Channel routing occurs as nature problem in standard cell and building block layout styles. But also in the design of printed circuit boards(PCBs)

10. Define area routing.

Routing problems in which terminals are allowed anywhere in the area available for routing are normally classified as area routing problems.

11. What are the channel routing models?

1. All wire run along orthogonal grid lines with uniform separation
2. There are two wiring layers.
3. Horizontal segments are put on one layer and vertical segments on the other one.

12. Define doglegs. (MAY 2012)

The use of doglegs, i.e, of more than one horizontal segment per net, often offers the possibility of channel height reduction.

13. What is global routing?

Global routing decides about the distribution across the available routing channels of the interconnections as specified by a net list.

14. What is the use of feed through cells. (NOV 2010)

These are cells that are inserted between functional cells in a row of standard cells with the purpose of realizing vertical connections. By making use of feed through wires that may be available within standard cells.

15. Write the advantages of divide and conquer algorithm. (MAY 2007)

Limited problem size at each level of recursion
Completely independent

16. Write the goal of global routing.

The goal of global routing is to minimize the total channel density
Maximum number of feed through cells.

PART – B

1.i) Explain the floor planning concepts in detail.
ii) Explain the optimization problems in floor planning. (MAY 2008, MAY 2010,NOV 2009)
2..i) Explain the shape functions and floor plan sizing in detail.
ii) Explain the types of local routing problems. (NOV 2007)
3. Explain in detail about global routing.
4. Explain in detail about area and channel routing with an example. (MAY 2011)
5. Differentiate area and channel routing. (NOV 2009)
6. Explain the algorithm for global routing with an example. (NOV 2010,MAY 2012)
7. Brief about floor planning and routing mechanisms. (MAY 2011)

UNIT: IV – SIMULATION AND LOGIC SYNTHESIS

PART-A

1. Define simulation. (MAY 2012)

A process of design verification is simulation. It is extremely costly to repair design errors after the fabrication of an integrated circuit, one needs to have sufficient confidence that all design errors have been eliminated before delivering the design to the foundry.

2. What are the two ways to verify a design? (NOV 2010, MAY 2009)

1. By simulation
2. By formal verification

3. What are the different types of simulation? (MAY 2011)

1. Device - level simulation
2. Circuit - level simulation
3. Timing - level and macro - level simulation
4. Switch - level simulation
5. Gate - level or logic - level simulation
6. Register - transfer-level (RTL) simulation

4. What are the software modules that generally constitute a simulator?

1. The simulator kernel
2. The processing of the input description
3. The processing of the stimuli
4. The presentation of the results.

5. What are the types of gate – level modeling? (MAY 2011)

1. Signal modeling (correspondence between voltage and current values in the real circuit and the discrete signals in the model)
2. Gate modeling (the representation of a gate's behavior)
3. Delay modeling (the various types of delays encountered at the gate level)
4. Connectivity model (the representation of the interconnections between the gates)

6. What are the types of delay modeling? (NOV 2012)

1. The propagation delay model (zero and unit delay model)
2. The rise/fall delay model
3. The inertial delay model

7. Compare compiler-driven and event -driven simulation (MAY 2011, NOV 2010)

Compiler driven simulation: best choice occurs in the context of synchronous circuits. The core of such a circuit consists of that store the state of the system and combinational logic that computes the next state.

Event driven simulation: motivated by the fact that normally very few gates are switching simultaneously and that computing signal propagation through all gates in the network over and over again at each time instant, as in compiler -driven simulation amounts to many unnecessary calculations.

8. How the signal can be represented in switch level modeling?

A signal is represented by a pair (s,v) where s is a strength, v is a level ,a voltage with discrete values at least including '1','0'and'x' where 'x' represents the unknown signal value.

9. What is storage nets?

That are able to store charge, they have a strength (capacitance value) which is discrete.

10. How the transistors are modeled in switch level simulation?.

At the switch level, signals are discrete, but signal flow is bidirectional due to switches that model the transistors. Transistors are the only electrical components of which a circuit at the switch level is composed except for resistances and capacitances that may also be included in the circuit model for a better approximation of a real circuit behavior.

11. Compare static partitioning and dynamic partitioning. (MAY 2013)

Static partitioning in which connections to the gate of a transistor determine sub circuit boundaries irrespective of the signals carried by the nets.

Dynamic partitioning takes signal values into account which can result in a further partitioning of the sub circuits.

12. Define Multi graph. (MAY 2012)

Graph model with a single type of vertex for the nets and one type of edge for the transistors. The edge runs between the net connected respectively to the source and gate ports of the transistor. The resulting graph is a multi graph, a graph in which parallel edges are allowed.

13. What is demand driven simulation? (NOV 2010, NOV 2011)

Instead of propagating stimuli forward through the circuit, it starts with the signals that the user wants to observe in sometime interval and goes backwards towards the circuit inputs.

14. Define priority queue.

A priority queue can deal with events spanning any time scale (which means that time instances are not limited to small integer multiples of Δt).

15. Write the disadvantages of event driven simulation. (MAY 2012)

The data structure can both return the earliest event and add new events in constant time. Of course, the solution has one huge disadvantage: It requires that the array is as big as the number of time steps that the simulation should take.

16. Define unit delay model. (NOV 2010,MAY 2011)

A model that is slightly more realistic than the zero - delay model is the unit - delay model in which the signals take one unit of time to propagate from the inputs to the outputs of any gate.

17. How the event queue will store the events? (NOV 2010)

By following two actions

1. Returning the earliest of the events still to be processed and removing it from the queue.
2. Adding a new event at an arbitrary time in the queue.

18. Define Message Queue.

A message queue is a buffer managed by the operating system. Message queues allow a variable number of messages, each of variable length, to be queued. Tasks and ISRs can send messages to a message queue, and tasks can receive

messages from a message queue (if it is nonempty). Queues can use a FIFO (First In, First Out) policy or it can be based on priorities. Message queues provide an asynchronous communications protocol.

PART – B

1. Explain in detail about abstraction levels for simulation. (MAY 2011)
2. Explain the software modules of simulation.
3. Explain in detail about gate level modeling and simulation with example.(NOV 2012,MAY 2010)
4. Explain the types of delay modeling in detail.
6. Explain in detail about switch level modeling and simulation with example.(MAY 2012,NOV 2010)
7. Write the pseudo code of a switch level simulation algorithm. (NOV 2011,MAY 2013)
8. Compare event driven and compiler driven simulation in detail.
9. Explain the simulation mechanisms of switch level modeling. (MAY 2012)

UNIT:V – HIGH LEVEL SYNTHESIS

PART-A

1. Define logic synthesis. (NOV 2011)

The automatic generation of circuitry starting from bit- level descriptions is known as logic synthesis. Purpose of checking the solution's correctness is ensured by synthesis.

2. What is on set and off-set? (MAY 2009,MAY 2011)

On - set: contains all points for which the output should be '1'
Off - set: contains all points for which the output is '0'

3. What is literal? (MAY 2010)

The term literal denotes a Boolean variable or its complement

4. Define minterm. (MAY 2012)

Any point in B^m can be identified by a product of m distinct literals. Such a product is called a minterm.

5. What is ROBDD?

The sum of minterm representation suffers from not being compact. So an alternative is introduced called reduced order binary-decision diagram (ROBDD).It is widely used for logic synthesis and verification.

6. What will be the output for the input signals in logic synthesis? (NOV 2009, MAY 2010)

1. On-set
2. Off-set
3. Dont care

7. Define cube.

The booolean variable associated with the absent literal can have both possible Boolean values. The set of points defined in this way is called a cube.

8. Give Shannon expansion of a Boolean function. (MAY 2012)

The two restrictions with respect to a single Boolean variable are used to express the identity which is known as the Shannon expansion of a Boolean function f.

$$f = x_i.f_{xi} + x_i(bar).f_{xi}(bar)$$

9. How size reduction of an OBDD is done in order to obtain an ROBDD?(NOV 2013, MAY 2010)

i) Replace all leaf vertices v with identical Φ(v) by a single vertex and redirect all edges incident to the original vertices to this single vertex.
ii) Process all vertices from bottom to top.
iii) If edges v exist for which η(v)=λ(v) and redirect to η (v) all edges originally incident to v.

10. Define hash table. (NOV 2010, MAY 2011)

It has the nice property that it can return an entry in constant time without needing to reserve storage space for all possible entries.

11. What is composition problem? (MAY 2010)

A frequently encountered problem is to construct the ROBDD of a combinational circuit build of discrete components , the so- called composition problem.

12. What are the basic functions of garbage? (NOV 2011)

BDD packages use so called garbage collection mechanism to automatically remove vertices that are no longer required.

13. What are the applications of verification? (MAY 2009)

It checks whether a combinational logic circuit that resulted from manual or automatic (but possibly erroneous) logic synthesis, the so called implementation, obeys the specification of the circuit.

14. How quine Mc Cluskey algorithm works?

The algorithm first generates all prime implicants of the union of on-set and dc-set omitting those prime implicants that only cover point of dc-set. It then finds the minimum cost cover of all min terms in the on-set by prime implicants from the set of all primes.

15. What is row dominance?

If for some row s_i in a covering matrix all columns by which it is covered cover another row s_j ,it is said that s_i dominates s_j. s_j can be removed from the covering matrix due to row dominance.

16. What is column dominance?

If all rows covered by some column k_j are covered by column k_i, it is said that k_i dominates k_j. k_j can be removed from the covering matrix due to column dominance.

PART – B

1. Explain in detail about the heuristics based on ROBDD.(MAY 2012,NOV 2010)
2. Explain briefly about the various applications of combinatorial optimization.
3. Explain in detail about two level logic synthesis with an example. (MAY 2010)
4. Explain various applications of verification.
5. Explain the ROBDD manipulation in detail.(NOV 2012,MAY 2011)
6. Give the ROBDD principles and explain the reduction from OBDD to ROBDD. (NOV 2010)
7. Explain the principles involved in combinational logic synthesis.
8. Explain how ROBDD can be constructed and implemented. (MAY 2012)