



## QUESTION BANK

Name of the Department : **Electronics and Communication Engineering**

Subject Code & Name : **II4092 & System on Chip**

Year & Semester : **I & II (M.E-VLSI Design)**

### UNIT – I

#### SYSTEM ARCHITECTURE: OVERVIEW

##### PART – A

#### **1. Define Memory in SoC.**

Memory in a system on a chip (SoC) is a collection of semiconductor memory blocks that stores instructions and data for the SoC to perform computations.

#### **2. What is addressing in SoC?**

Addressing in a System-on-a-Chip (SoC) refers to the internal connections of components on a single chip. SoCs are integrated circuit (IC) designs that combine many of an electronic device's functions onto a single chip, instead of using separate components on a motherboard.

#### **3. Define system level interconnection.**

System level interconnection in a System on a Chip (SoC) is the connection between different components of the SoC. This connection allows for efficient communication and data transfer between the components.

#### **4. Define design integration.**

Design integration in System-on-a-Chip (SoC) refers to the process of integrating multiple processing elements into a single chip

#### **5. What do you meant by SoC?**

An SoC is an integrated circuit that combines many of an electronic device's components onto a single chip.



## **6. What is meant by design complexity?**

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Design complexity is the level of intricacy and sophistication in the design of a system or application.

## **7. List the SoC design requirements.**

Processor cores, Memory, Interfaces, Timing sources, Quality, Performance, Power consumption, Subsystems, Design workflow.

## **8. What is SoC specification?**

Along with a processor, the SoC usually contains a GPU (graphics processor), memory, USB controller, power management circuits, and wireless radios.

## **9. List the applications of SoC.**

Mobile devices: SoCs integrate wireless connectivity and multimedia capabilities in smartphones and tablets. Automotive systems: Vehicles of all types use SoCs to power navigation systems, sensor interfaces, infotainment systems, and danger avoidance systems.

## **10. What is cycle time?**

Cycle time is a metric that measures the time it takes to complete a process or operation, and it can be used in software development.

## **11. Define configurability.**

Configurability in System-on-a-chip (SoC) design can help reduce costs, broaden applicability, and improve productivity.

### **PART – B**

1. Explain the components of the system with a neat diagram.
2. Write short notes on SoC design requirement and specification.
3. Explain about memory and addressing with neat sketch.
4. Describe about system level interconnection.
5. Write short notes on design integration and design complexity.



## UNIT II

### PROCESSOR SELECTION FOR SOC

#### PART – A

##### **1. Specify the processor core selection.**

Processor core selection in a system on a chip (SoC) is the process of choosing the processor cores that will be used in the SoC.

##### **2. Define soft processors.**

A soft processor, also known as a soft core processor, is a CPU design that can be synthesized within a programmable logic device, such as a field programmable gate array (FPGA).

##### **3. What is robust processor?**

A robust System-on-a-Chip (SoC) is one that can continue to function reliably despite the presence of faults.

##### **4. What is vector processor?**

A vector processor is a central processing unit (CPU) that executes instructions on arrays of data, instead of single data elements. Vector processors are also known as array processors.

##### **5. Define instruction handling.**

Instruction handling in a system on a chip (SoC) is the process of executing instructions that a computer program provides to a computer processor.

##### **6. What is the purpose of superscalar processor?**

A superscalar processor is a type of microprocessor that can execute multiple instructions at once, without interrupting the program's algorithm or result.

##### **7. What is meant by VLIW processor?**

A Very Long Instruction Word (VLIW) processor is a CPU architecture that allows programs to explicitly specify which instructions to execute in parallel. VLIW processors are used in high-performance embedded applications and some high-performance servers.

##### **8. Define pipeline delays.**

It represents delay or time it takes for an instruction to pass through pipeline stages. Lower latency indicates better performance.



## 9. What is meant by branches?

A branch is an instruction in a computer program that causes the computer to start executing a different sequence of instructions. In a System-on-a-Chip (SoC), branches are used to implement control flow in program loops and conditionals.

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## 10. Define instruction set.

An instruction set is a collection of machine language commands that a computer's processor can understand and execute.

### PART - B

1. Explain on soft processors in detail.
2. Discuss in detail about basic elements in instruction handling.
3. Write short notes on instruction sets and interrupts in SoC.
4. Explain about how to minimize pipeline delays in detail.
5. Discuss in detail about robust processors.



## UNIT III

### MEMORY DESIGN

#### **1. What is SoC external memory?**

In a system on a chip (SoC), the external memory interface enables the processor to connect with external memory, peripherals, and third level caches.

#### **2. Define SoC internal memory.**

Internal memory, also known as primary or main memory, is the memory in a system on a chip (SoC) that stores small amounts of data that can be accessed quickly.

#### **3. What is scratch pads?**

Scratchpad memory (SPM) is a type of high-speed, internal memory in a system on chip (SoC) that's used to temporarily store data and calculations.

#### **4. Define cache memory.**

Cache memory is a type of temporary memory in a computer that stores frequently used data and instructions for faster access by the CPU. It's a vital component of computer systems, and it's used to improve system performance.

#### **5. Write about split-I cache.**

Instruction cache: Also known as the I-cache, this cache stores instructions.

#### **6. What is split-D cache?**

Data cache: Also known as the D-cache, this cache stores data.

#### **7. What is multilevel caches?**

A multilevel cache, also known as a cache hierarchy, is a memory architecture that uses multiple levels of memory to store data based on access speed. The goal of multilevel caching is to allow the central processing unit (CPU) to access data faster, which can improve system performance.

#### **8. Define SoC memory system.**

The memory system in a system on a chip (SoC) includes memory blocks, a memory scheduler, a memory controller, and DRAM memory.

#### **9. Define cache organization.**

Cache organization refers to the logical arrangement of data in a cache, which is a small, fast memory that stores a copy of the main memory's contents.



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## 10. What is meant by board based memory system?

A board-based memory system is a hardware concept that includes different types of memory and electrical elements, such as ROM, RAM, flash memory, and auxiliary memory.

### **PART – B**

1. Describe the external and internal memory in SoC in detail.
2. Explain about scratch pads and cache memory.
3. Discuss about multilevel caches in detail.
4. Discuss on SoC memory systems in detail.
5. Write short notes on simple processor/memory interaction.





**PART – A**

**1. What is bus?**

A bus in a system on a chip (SoC) is a backbone that carries signals, including address, data, command, and synchronization signals, to enable communication between components within the SoC.

**2. What is SoC standard bus?**

The bus is a collection of signals (wires) to which one or more IP components (which need to communicate data with each other) are connected.

**3. What is AMBA?**

Advanced Microcontroller Bus Architecture (AMBA) is an open standard for managing and connecting functional blocks in a system-on-chip (SoC). AMBA is royalty free, platform independent, and can be used with any processor architecture.

**4. What is core connect?**

Core connect is a microprocessor bus architecture for system-on-a-chip (SoC) designs that helps make it easier to integrate and reuse processor, system, and peripheral cores. It's a standard SoC design point that's used by IBM and other companies.

**5. Write about reconfigurable technologies.**

Reconfigurable technologies in system-on-chip (SoC) are used to customize a system after manufacturing, allowing it to be adapted for different computations.

**6. What is FPGA?**

A Field Programmable Gate Array (FPGA) is a versatile integrated circuit that can be reprogrammed after manufacturing to suit different purposes.

**7. What is FPGA memory?**

Field-programmable gate arrays (FPGAs) are integrated circuits (ICs) that can be reconfigured after manufacturing to meet specific requirements. FPGAs contain memory elements, such as flip-flops or more complex memory blocks, within their logic blocks.

**8. Define floor plan.**

In FPGA, a floor plan is a set of physical constraints that control the placement of logic on the die. It's a crucial step in the design process that determines the layout of the VLSI



design. A well-optimized floor plan can improve the quality of timing results and reduce routing congestion. }  
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## **9. List applications of FPGA.**

Embedded system, Radar system, Signal processing and cyber security.

## **10. Define routing.**

Routing in a field-programmable gate array (FPGA) is the process of designing the wires that connect the various components on the FPGA grid.

## **PART – B**

1. Describe on bus architectures in detail.
2. Discuss on AMBA.
3. Discuss about architecture of FPGA in detail.
4. Explain in detail about FPGA interconnect technology.
5. Write short notes on reconfigurable technologies.





## UNIT V

### FPGA BASED EMBEDDED PROCESSOR

#### PART – A

##### **1. What is task partitioning?**

Task partitioning in an FPGA (Field Programmable Gate Array) is the process of dividing the FPGA space into slots to share resources between multiple tasks. The goal of partitioning is to balance FPGA utilization and minimize interconnect.

##### **2. What is hard processor?**

A hard processor in an FPGA is a commercial, proprietary processor that's integrated into the same chip as the FPGA fabric.

##### **3. What is soft processor in FPGA?**

A soft processor in an FPGA is a microprocessor core that is implemented in the logic primitives of a Field Programmable Gate Array (FPGA). It is a hardware description language (HDL) model of a specific processor that can be customized and synthesized for an FPGA.

##### **4. What is the need for wishbone interface?**

The Wishbone System-on-Chip (SoC) Interconnect Architecture is a free, open-source standard that defines a common interface between IP cores in an FPGA. It's a portable interface that's independent of the underlying semiconductor technology.

##### **5. What is FPGA based embedded processor?**

An FPGA-based embedded processor is a system that uses a field-programmable gate array (FPGA) to execute code in hardware. FPGAs are integrated circuits that can be reprogrammed to add or change functions, and are often used for high-compute tasks in embedded systems.

##### **6. Define Avalon switch matrix.**

The Avalon interface family defines interfaces appropriate for streaming high-speed data, reading and writing registers and memory, and controlling off-chip devices.

##### **7. Define OPB bus interface.**

The On-Chip Peripheral Bus (OPB) is a bus specification that's used in FPGAs to connect slower devices. It's a synchronous, non multiplexed, multimaster, arbitrated bus with a 64-bit address bus and separate 32-bit read and write buses.



## **8. What is FPGA based signal interfacing?**

FPGA-based signal interfacing is a method of using Field Programmable Gate Arrays (FPGAs) to process signals and perform other tasks. 10

## **9. Define FPGA based conditioning.**

FPGA-based conditioning is a type of conditioning that uses a Field Programmable Gate Array (FPGA).

## **10. List the applications of FPGA based embedded processor.**

Digital signal processing, Medical electronics, Image and video processing and Data centers.

### **PART – B**

1. Brief about soft processors and hard processors.
2. Explain on types of on-chip interfaces in detail.
3. Explain in detail FPGA fabric immersed processors.
4. Describe on tool flow for hardware/software co-design.
5. Explain FPGA based signal interfacing and conditioning.