QUESTION BANK

Name of the Department : Electronics and Communication Engineering. M.E VLSI Design

Subject Code & Name : VL4291 & Low Power VLSI Design

Year & Semester : I & II

UNIT – I

POWER DISSIPATION IN CMOS

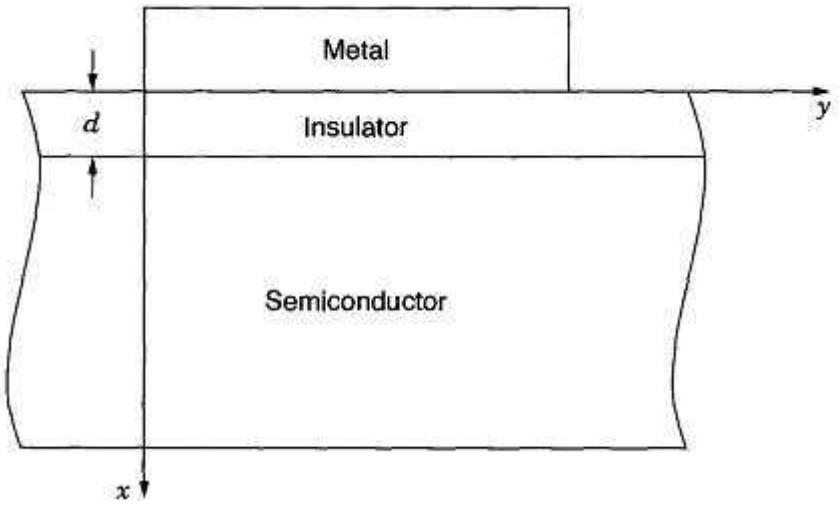
PART – A

1. What are the sources of power consumption in CMOS circuits?

There are three sources of power dissipation in CMOS circuits.The first source are the logic transitions. Short-circuit currents that flow directly from supply to ground when the *n-subnetwork* and the *p-subnetwork* of a CMOS gate both conduct simultaneously are the second source of power dissipation. The third and the last source of dissipation is the leakage current that flows when the input(s) to, and therefore the outputs of, a gate are not changing.

2. What is MIS structure? Draw the basic MIS structure.

The metal-insulator-semiconductor (MIS) structure besides being a device (a voltage variable capacitor and a diode), is an excellent tool for the study of semiconductor surfaces.



3. When does the flat band condition occur in an unbiased MIS diode structure?

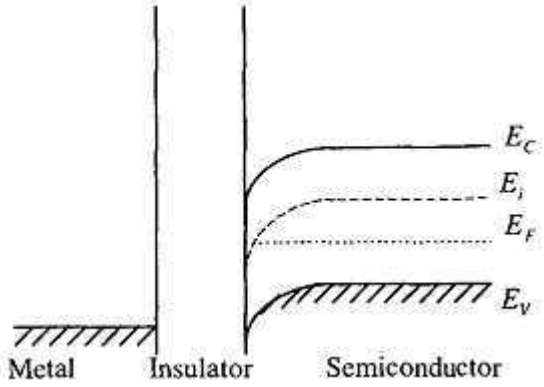
In an ideal MIS diode the insulator has infinite resistance and does not have either mobile charge carriers or charge centers. As a result, the Fermi level in the metal lines up with the Fermi level in the semiconductor. The Fermi level in the metal itself is same throughout (consequence of the assumption of uniform doping). This is called the flat-band condition.

4. What is meant by weak inversion?

When the applied voltage V is positive but small, the holes in the *p-type* semiconductor are repelled away from the surface and leave negatively charged acceptor ions behind. A depletion region, extending from the surface into the semiconductor, is created. This is the *depletion* condition. Besides repelling the holes, the positive voltage on the gate attracts electrons in the semiconductor to the surface. The surface is said to have begun to get *inverted* from the original *p-type* to *n-type.* While V is small, the concentra- tion of holes is still larger than the concentration of electrons. This is the *weak-inversion* condition and is important to the study of power dissipation in MOSFET circuits.

5. How does the strong inversion occur?

The electron density at the surface is still smaller than the hole density deep inside the semiconductor. When V is increased to the extent that the electron density at the surface n_s becomes greater than the hole density ($\approx N_A$, the concentration of acceptor impurities) in the bulk, onset of *strong inversion* is said to have occurred. This condition is depicted in Figure.



6. Define threshold voltage with respect to strong inversion.

The value of V necessary to reach the onset of strong inversion is called the *threshold voltage.*

7. Define work function.

The work function is defined as the minimum energy necessary for a metal electron in a metal-vacuum system to escape into the vacuum from an initial energy at the Fermi level.

8. What is V_{FB}?

The total voltage needed to offset the effect of nonzero work function difference and the presence of the charges is referred to as the *flat-band voltage* V_{FB}.

9. Give the equation for the depth of depletion region of a semiconductor.

$$\sqrt{\frac{2\phi_s \varepsilon_s}{qN_A}} = W$$

Where, N_A is the concentration of acceptor impurities,

ϕ_s is the potential at the surface,

ε_s is the permittivity of the semiconductor medium.

10. What is meant by punchthrough effect?

$$I_{D,\text{st}} = D_n Z \frac{\partial Q_i(y)}{\partial y} = \frac{qD_n Z}{L} \frac{\beta\sqrt{\varepsilon_i}}{\sqrt{2qN_A\phi_s(y=0)}} \frac{n_i^2}{N_A} e^{q\beta\phi_s(y=0)}$$

It is seen that in long-channel MOSFETs, the subthreshold drain–source current remains independent of the drain–source voltage. As $\phi_s(y = 0)$ varies exponentially with the applied gate voltage [3], so does the drain–source current. The independence of $I_{D,\text{st}}$ from V_{DS} ceases even in MOSFET with L as large as 2 μm when V_{DS} is large enough that the source and drain depletion regions merge. This short-channel effect is called *punchthrough.*

11. What do you know about subthreshold swing?

The inverse of the slope of the log $I_{D,\text{st}}$ versus V_{GS} characteristic is called the *subthreshold swing*. For uniformly doped MOSFETs,

$$S_{\text{st}} = \log\left(\frac{d \ln I_D}{dV_{GS}}\right)^{-1} = 2.3\beta\left(1 + \frac{C_d}{C_{\text{ax}}}\right) = 2.3\beta\left(1 + \frac{\varepsilon_s d}{\varepsilon_i W}\right)$$

where C_d is the capacitance of the gate depletion layer, C_i the capacitance of the insulator layer, ε_s the permittivity of the semiconductor, ε_i the permittivity of the insulator, d the thickness of the insulator, and W the thickness of the depletion layer.

12. List out the effects influencing threshold voltage in a submicron MOSFET.

i) Short-Channel-Length Effect
ii) Drain-induced barrier lowering (DIBL)
iii) Narrow Gate Width Effects
iv)Reverseshort-channeleffect

13. How the Gate Induced Drain Leakage(GIDL) current is controlled in MOSFETs?

In CMOS circuits this leakage cur- rent contributes to standby power. The GIDL can be controlled by increasing the oxide thickness (reducing the field for a given voltage), increasing the doping in the drain (to limit the depletion width and the tunneling volume), or eliminating traps (assuming voltages and fields low enough that trap-free band-to-band tunneling is not possible).

14. What is meant by static power dissipation?

The NMOS inverter dissipates significant amount of power even when its input is not changing. For this reason this component of power dissipation is called *static* power dissipation.

15. List the advantages and disadvantages of CMOS over NMOS with respect to static power dissipation.

Static power dissipation in CMOS is due to leakage currents and is small in comparison to other components. This advantage of CMOS over NMOS has proven to be important enough that the shortcomings of CMOS are overlooked. The CMOS process is more complex than the NMOS, the CMOS requires use of guard-rings to get around the latch-up problem, and CMOS circuits require more transistors than the equivalent NMOS circuits.

16. What are the facts about dynamic component of power dissipation?

Two facts about the dynamic component of power dissipation are of interest: **It** is by far the
dominant component and it is proportional to the product of load capacitance C_L and the square of the supply voltage V_{dd}. Hence reduction of dynamic power voltages V_{Tn} and V_{Tp} become critical parameters.

17. Mention the characteristics of short circuit power dissipation of an unloaded inverter.

If the input and the output signal have equal rise and fall times, the short-circuit dissipation is small. However, if the inverter is lightly loaded, causing output rise and fall times that are relatively shorter than the input rise and fall times, the short-circuit dissipation increases to become comparable to dynamic dissipation. Therefore, to minimize dissipation, an inverter should be designed in such a way so that the input rise and fall times are about equal to the output rise and fall times.

18. Give the relationship for the dynamic power dissipation of CMOS inverter.

$$P_D = \frac{C_L V_{DD}^2}{T}$$

19. Tabulate the average gate capacitance of a MOS transistor in the Three regions of operation.

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{exx}$	0	0
Triode	0	$C_{ox}WL_{exx}/2$	$C_{ox}WL_{exx}/2$
Saturation	0	$(2/3)C_{ox}WL_{exx}$	0

20. State the principles of low power design.

There are three key principles of low-power design: (1) using the lowest possible supply voltage, (2) using the smallest geometry, highest frequency devices but operating them at the lowest possible frequency, (3) using parallelism and pipelining to lower required frequency of operation, (4) power management by disconnecting the power source when the system is idle, and (5) designing systems to have lowest requirements on subsystem performance for the given user level functionality.

21. What are the hierarchy of limits of power?

A hierarchy of limits that has five levels: (1) fundamental, (2) material, (3) device, (4) circuit, and (5) systems. At each level two types of limits exist: (1) from theoretical considerations and (2) from practical considerations.

PART – B

1. Explain the various sources of dynamic power dissipation in CMOS circuits?
2. What are the trade-offs involved in low power VLSI design?
3. Explain the sources of leakage power and the methods to reduce it.
4. State the principles of low power VLSI design.
5. Derive an expression for the average dynamic power dissipation in CMOS.
6. Explain the various limits of power in VLSI circuits.
7. Explain the physical parameters of MOSFET which affect the various sources of power dissipation.

UNIT II

POWER OPTIMIZATION

PART – A

1. Classify the technology independent optimization techniques concerning the circuit type.

i. Optimization techniques for combinational class

ii. Optimization techniques for sequential class

2. What are the techniques for optimizing multilevel combinational circuits in terms of area and delay?

i. Boolean optimization techniques

ii. Algebraic techniques.

3. Mention the advantage of using guarded evaluation technique for the implementation of shut down mechanism.

It is a shutdown technique that does not require to synthesize additional logic to implement the shut down mechanism.

4. What do you know about logic optimization technique based on pre-computation?

This optimization technique is based on selectively pre-computing of the output logic values of a circuit one clock cycle before they are required and then use the pre-computed values to reduce the internal switching activity of the combinational logic in the successive clock cycle.

5. What is the main difference between power optimization at various abstract levels?

The main difference between power optimization at different levels of design abstraction is the trade-off between computing resources and accuracy of results. Even though System/Algorithm/Architecture level power optimization techniques have a large potential for power saving, these techniques tend to saturate as more functionality is integrated on the IC. Hence optimization at logic/circuit/device level is also very important for the miniaturization of IC.

6. What are the advantages of path balancing in a technology dependent optimization.

- Selectively collapsing the fan-ins of the node
- Logic decomposition and extraction can be performed
- Inserting variable delay buffers in a circuit

7. What is meant by technology decomposition?

It is the next step during the logic synthesis of a network. It is the conversion process of the network to another which only contains a two input AND / NAND and inverter gates. This step is called technology decomposition. It is very useful for network synthesis and is carried out before the mapping of the network according to the current cell library.

8. What are the steps involved in the technology mapping process?

(i) The first step requires the computation of power delay curves of all nodes in the network.

(ii) The second step produces the mapping solution according to the previous curves.

9. Write briefly about the advantage of using post mapping optimization over technology independent optimization.

The major drawback of low power technology independent optimization is that the estimation of power consumption which is used to guide the optimization of the Boolean network is inaccurate. This arises from the fact that the final structures of the circuit and load capacitance of each node are unknown. On the other hand the post mapping optimization allows performing power and timing analysis on the mapped circuit which provides more realistic estimates.

10. State the scope of the logic style for the circuit level low power design.

The scope of the logic style for the low power design at circuit level is to introduce the basic logic styles for designing digital integrated circuits on speed, size and power consumption.

11. What are the characteristics of static logic under circuit level low power design?

(i) Ratioless logic (ii) High noise margins which offer low sensitivity to noise (iii) Sufficient speed especially for small gates. (iv) Comparable rise and fall times under appropriate scaling (v) Ease of design.

12. List the power considerations of circuit level low power design.

(i) Dynamic power (ii) Short circuit power (iii) Leakage power

13. Why the dynamic logic style is preferred in CMOS circuits during low power design?

Dynamic logic is often used in CMOS circuits to reduce the transistor count to increase the speed and to avoid static power consumption.

14. How will you overcome the problem of cascading dynamic gates during power consideration for low power design at circuit level?

Two and four phase clocking strategies that have been developed to overcome the problem of cascading dynamic gates need upto 8 clock 0/1's and they are clearly not suited for low power operation. To correct the problem of cascading gates, the following strategies have been proposed. These are:

(i) Domino(7) (ii) NP-CMOS(8) (iii) NOR A(9)

15. What are the advantages of Single Rail Pass Transistor logic?

(i) The single ended pass transistor logic has no more than ten components. Basically it has only three main components.

(ii) The pass transistor network contains only NMOS transistors resulting in a compact layout with fast open.

16. When do you prefer Pseudo nMOS logic style?

The pseudo nMOS logic style is alternative when designing complex gates with large fan-ins, because the pull up network is replaced by a single load resistor. It requires smaller area and smaller parasitic capacitance. Pseudo nMOS can reduce power consumption for complex logic

functions switching at high frequencies where savings to the dynamic power component due to reduced capacitances are dominant.

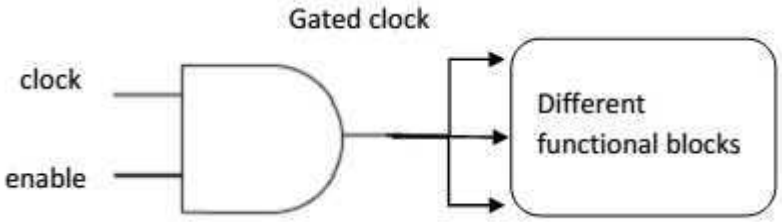
17. Describe the advantage of using differential voltage logic style over pseudo nMOS logic style.

(i) Faster switching due to reduced output capacitance
(ii) No static power consumption

18. Mention the different static and dynamic latches available for designing low power circuits.

(i) C2MOS latch (ii) True single phase clocked half cycle (iii) cascode voltage switch logic
(iv) Dynamic single transistor clocked (v) TGATE (vi) n-RAM

19. What do you know about clock gating?



Clock gating is a widely accepted technique in the industry which disables clock to idle portions of the chip, thereby avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In clock gating, clock is selectively stopped for portions of circuit which are idle, by using an enable signal.

20. What do you know about transistor ordering?

The relative placement of the transistors in a serially connected MOSFET chain does not alter the functionality of the chain in the circuit. In complex gates where groups of transistors may be connected in in series, flexibility also often exists in the relative placement of the transistor. With a set of simple transistor reordering rules, 10 % reduction in power consumption can be achieved.

21. What do you know about transistor sizing?

Appropriate sizing of the transistor in CMOS circuits can be applied for minimizing the power consumption under a given delay constraint.

(i) Algorithms that start by performing an initial power optimal sizing on each gate. If the power minimal layout satisfies the delay constraint, the process is terminated, otherwise the power delay optimal sizing is applied to transistor sizes on the critical paths until the timing target is met.
(ii) Algorithms that start with a circuit that satisfies the timing constraint and reduce the size of the gate to reduce power optimization.

This algorithm is more complex because it takes into account not only the power dissipation which is due to the charging of the circuit capacitance but also the short circuit power dissipation.

22. What are the eight important designs in CMOS logic style?

- Conventional Static CMOS – CSL
- Complementary Pass Transistor – CPL
- Double Pass Transistor – DPL
- Static and Dynamic Differential Cascode Voltage Switch – DCVSL
- Static Differential Split-Level – SDSL
- Dual-Rail Domino – DRDL
- Enable/Disabled CMOS Differential – ECDL
-

23. State the advantage of using CPL logic over CSL logic.

CPL circuits consume less power than conventional static circuits because the logic swing of the pass transistor outputs is smaller than the supply voltage level.

24. What is the operation of DPL logic?

DPL is a modified version of CPL. In DPL circuits, full swing operation is achieved by simply adding pMOSFET transistors in parallel with the nMOSFET transistors. Hence, the problems of noise margin and speed degradation at reduced supply voltages which are caused in CPL circuits due to reduced high voltage level, are avoided. However, the addition of pMOSFETs results in increased input capacitances.

25. What are the merits and demerits of SDSL full adder circuit?

Merit: Faster circuit operation than standard DCVSL circuits.

Demerits: Due to incomplete turn-off of the cross-coupled pMOSFET transistors, SDSL circuits dissipate high static power dissipation. Also, the addition of two extra nMOSFET transistors per gate results in area overhead.

26. What is the purpose of using Dual-Rail Domino Logic?

DRDL is a precharged circuit technique which is used to improve the speed of CMOS circuits.One major advantage of the dynamic, precharged design styles over the static styles is that they eliminate the spurious transistions and the corresponding power dissipation. Also, dynamic logic does not suffers from short circuit currents which flow in static circuits when a direct path from power supply to ground is caused.

27. What is the advantage of Dynamic Differential Cascode Switch Voltage Logic over Domino Logic?

The advantage of this style over domino logic is the ability to generate any logic function. Domino logic can only generate non inverted forms of logic.

28. What do you know about ECDL circuits?

Enable/Disabled CMOS Differential Logic is a self timed differential logic which is used in the case of implementing logic functions using iterative networks. It uses extra signals to indicate the beginning and ending of a function evaluation, in order to improve the circuit speed. One major advantage of the ECDL circuits is that there is no minimum clocking frequency requirement. However, ECDL circuits suffer from extra power dissipation due to the inverters which are needed to change the polarity of the output nodes. Also, their complex pull-up circuitry leads in extra silicon area.

29. Compare the different power saving circuit techniques of adders and multipliers.

The array multiplier is power efficient for small bit widths. Its power consumption grows in proportion to the cube of the word size. The Wallace multiplier is less regular, but is more power efficient, while its power dissipation grows with the square of the word size.

The speed of the synthesized optimized carry look-ahead is traded-off for the worst energy power consumption among all the investigated adders, which have been synthesized. As opposed to the speed optimized architecture of the carry look-ahead adder, a non-optimized architecture is power-efficient, though much slower. Power-efficient is the ripple carry adder, too.

PART – B

1. Explain the techniques used in logic-level power optimization.
2. How to optimize the static power of logic gate?
3. Explain the power optimization techniques used in adders.
4. What are the methods used to reduce switching activities in multipliers.
5. Explain in detail the circuit techniques to reduce the power consumption in adders and multipliers.
6. Explain the various methods of power optimization at the logic level.

UNIT III

DESIGN OF LOW POWER CMOS CIRCUITS

PART – A

1. **What do you know about the logarithmic number system for low power design?**
   Conventional arithmetic circuits and low power design techniques can be applied to realize components of VLSI architectures that implements logarithmic number system circuits. The logarithmic number system has been employed in the design of low power DSP devices. It is applicable for low power design because it reduces the strength of certain arithmetic operators and the bit activity. The operator strength reduction by logarithmic number system reduces switching capacitance.

2. **How does the Residue Number System(RNS) act for the design of low power circuits?**
   The RNS offers significant power dissipation savings in the design of similar processing architectures for FIR filters and frequency synthesizer. The RNS can reduce the power dissipation since it reduces the hardware cost, the switching activity and the supply voltage.

3. **What is static RAM?**
   These are read/write memory circuits which permit the modification of data bits stored in memory cells. Static means as long as efficient power supply voltage is provided the stored data is retained indefinitely. RAM means the access time is independent of the physical location of the data to be read/stored in the memory array.

4. **What are the sources of power dissipation in SRAMs?**
   Standby power consumption is due to leakage currents of the cross coupled CMOS inverters within each cell. This power component for state of the art SRAMs is usually negligible. Sources of active power consumption can be identified:
   - Driving lines with large capacitance
   - The memory array
   - The sense amplifiers which consume the largest portion of power.
   - Remaining peripheral circuits such as I/O buffers, write circuitry etc.
   -

5. **Write about the method of reducing word line selection delay of SRAM.**
   The increase in memory size in recent RAM technologies causes an unavoidable increase in word length. The memory array is divided into n sub arrays and each one is driven by a divided word line which is activated, the word line selection delay is reduced, improving memory speed.

6. **What are the advantages of using divided bit line approach for low power SRAM circuit?**
   The divided bit line approach is used to reduce power which is dissipated during read or write operation. 20-30% time is reduced and 50-60% power will be reduced. It uses original drain capacitance of n rows. This technique is used to avoid pass transistor in series by physically split bit lines.

7. What are the low power design techniques for sense amplifiers?

The role of sense amplifier is to detect the small differential static power from the bit lines when one line starts going low and amplify it. On the other hand the circuit of the sense amplifier itself consumes often the largest portion of the total power in an SRAM. Thus the cross coupled nMOS sense amplifier scheme achieves faster sensing and power reduction of approximately 20%.

8. State the principle of DRAM circuit?

The Dynamic RAM principle is to eliminate the load devices in each cell by simply storing binary data as a charge in a capacitor, whose state is periodically refreshed. It consists of one explicit storage capacitor and one access transistor.

9. List the sources of power dissipation in DRAMs?

- The row and column decoders
- The memory array which is the dominant source of power consumption in DRAMs.
- The sense amplifiers

10. What do you know about multi divided word line circuit technique?

In multi divided word line, the memory array is divided into several blocks and each block is divided into sub arrays. The sub word line circuitry embedded in each subway is responsible for selecting one sub word line at a time.

11. Write about an excellent technique to reduce the memory array power consumption in a DRAM.

An excellent technique to reduce the memory array power consumption in a DRAM is to pre-charge the bit lines to half V_{dd} instead of a full V_{dd} voltage employing a half voltage generator. It follows that a power reduction of about 50 % can be achieved together with area savings of about 30 % on-chip voltage down converter. The peak current for DRAM array can be more than 100 mA with transistor.

12. What are the factors to be considered for reducing clock power consumption?

- Hierarchical clock tree
- Careful design of the clock drivers to avoid the short circuit current.
- Minimum number of multiplexers connected to the clock.
- Frequency reduction by using double edge Flipflops.
- Multirate clocks
- Reduced swing for the clock distribution.

13. What is Adiabatic switching?

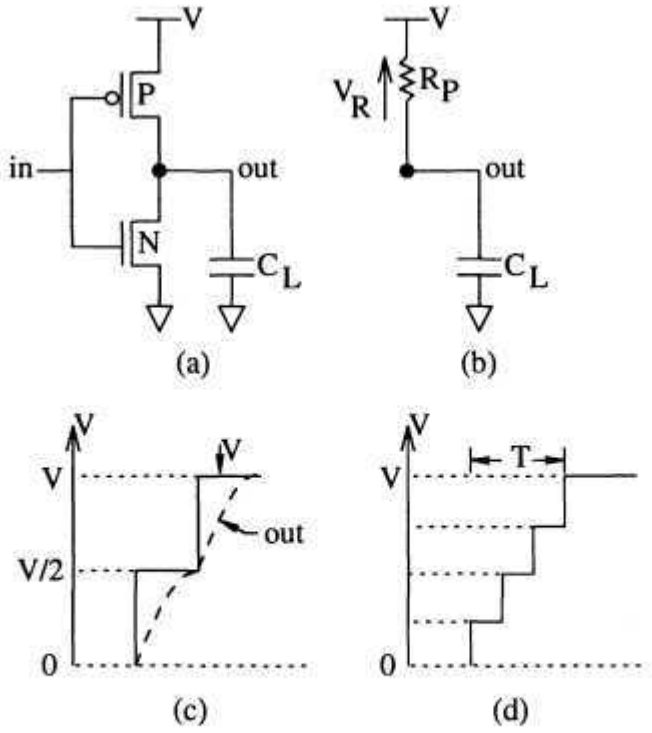


Figure 4.116 Adiabatic switching of an inverter (driver): (a) inverter; (b) equivalent charging circuit; (c) two-step power supply; (d) multi-step power supply.

The energy provided by the supply to charge a load C_L of a driver during charging and discharging is

$$E = C_L V^2$$

where V is the power supply voltage as shown in Fig. 4.116(a).

Half of the energy is dissipated by the resistor of the pull-up PMOS device during the charging phase. A similar argument applies to the discharge resistor of the pull-down NMOS transistor. This analysis is valid even if a step power supply voltage, V, is applied to the network. From Fig. 4.116(b), the voltage drop across the resistor, Rp varies from V (supply voltage) to zero. Hence, the energy dissipated by Rp is given by

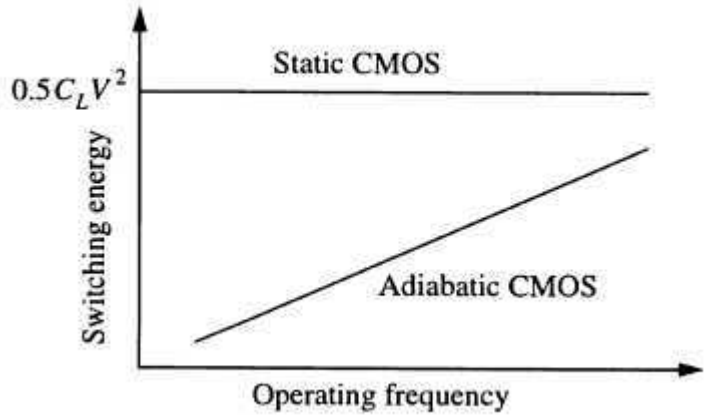
$$E_R = \frac{1}{2} C_L V^2$$

If the power supply voltage has two half steps, as shown in Fig. 4.116(c), the energy dissipated by the resistor is

$$E_R = \frac{1}{4} C_L V^2$$

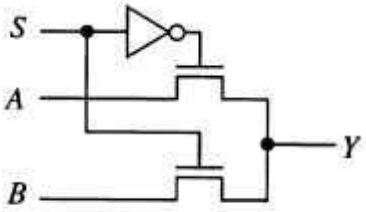
So less energy is dissipated by the resistor, when the average voltage is reduced, while keeping the swing and load capacitance constant. This is the principle of *Adiabatic Switching.*

14. Draw the switching energy transition graph of static CMOS and Adiabatic CMOS logic.



15. Write the basics of pass transistor logic with an example.

Pass transistor logic uses *pass transistors* to compose Boolean logic functions. A pass transistor is a MOS device that acts like a switch. It "passes" logic value from input to output when the device is turned on and isolates the input from the output when the device is turned off. An example of pass transistor logic implementing a two-input multiplexor is depicted in Figure. The select input turns on one of the pass transistors. This allows the input A or *B* to propagate to the output *Y* depending on the logic value of the select signal.

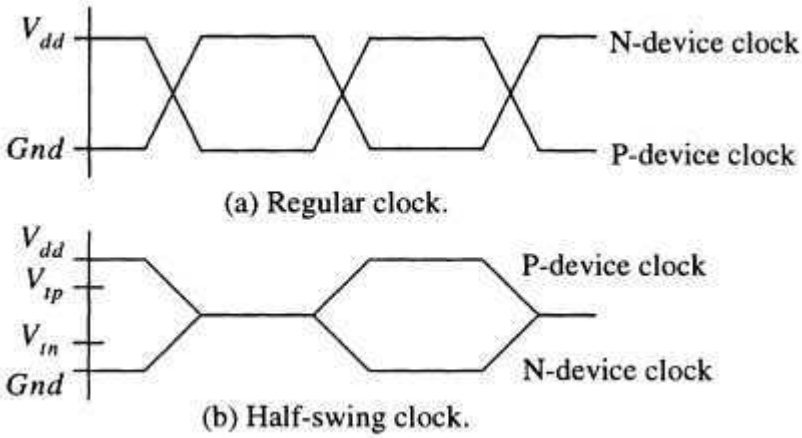


A two-input multiplexor using pass transistor logic

16. What is the purpose of using clock gating?

Clock gating, as depicted is the most popular method for power reduction of clock signals. When the clock signal of a functional module (ALUs, memories, FPUs, etc.) is not required for some extended period, we use a gating function(typically NAND or NOR gate) to turn off the clock feeding the module. Clock gating saves power by reducing unnecessary clock activities inside the gated module.

17. Draw the figure depicting Conventional and half-swing clocking scheme.



(a) Regular clock.

(b) Half-swing clock.

PART – B

1. Explain the organization of SRAM memory and the methods of power reduction used in it.
2. Explain the design of low power flip-flop circuits.
3. Explain the methods of power reduction in clock signals and buses.
4. Discuss how power saving is obtained using adiabatic computation.
5. Explain the techniques involved in reducing the power consumption in memories.
6. Explain in detail the computer arithmetic techniques for low power VLSI system.

UNIT IV

POWER ESTIMATION

PART – A

1. What is power estimation? What are the techniques present in estimating power?

Power estimation means, in general, the techniques of estimating the average power dissipation of circuits. Various power analysis techniques and tools are present at the circuit, gate, architectural, and behavioral levels of abstraction.

2. **Why estimate power dissipation?**

An accurate estimate of power dissipation during various phases of VLSI design can verify the power dissipation requirements and thereby avoid complicated and expensive design changes that might be required due to power constraint violations. Power estimates can also be used during the circuit, logic, and high-level synthesis to accurately trade off power versus other design parameters such as area, performance, and noise margin.

3. Why do glitches occur?

Power is also dissipated due to glitching activity in a circuit. Glitches occur due to different delays through different paths of the circuit.

4. What is signal gating? What are the different ways to implement signal gating?

Signal gating refers to a class of general techniques to mask unwanted switching activities from propagating forward, causing unnecessary power dissipation. Most signal gating techniques are applied at the logic level because switching activities of the signals can be easily analyzed.

There are many different ways to implement signal gating. The simplest method is to put an AND/OR gate at the signal path to stop the propagation of the signal when it needs to be masked. Another method is to use a latch or flip-flop to block the propagation of the signal. Sometimes, a transmission gate or a tristate buffer can be used in place of a latch if charge leakage is not a concern.

5. What do you know about switching activity of a sequential circuit model?

The switching activity of a sequential circuit is the sum of the switching activity of the primary inputs, primary outputs, internal node of the combinational circuit and nodes activity of the state lines.

6. How does the gate delay model affect the switching activity of a circuit?

One of the parameter that affects the switching activity of a circuit is the delay of the gates. The input signals of a gate may not arrive at the same time instance causing the gate output to perform spurious transistions.

7. Classify the power estimation methodologies.

Gate level power estimation → Simulation based → Advanced sampling
→ Monte-Carlo

→ Vector compaction
→ Probability based → Combinational circuits → Zero delay 17
→ Real delay
→ Sequential circuits

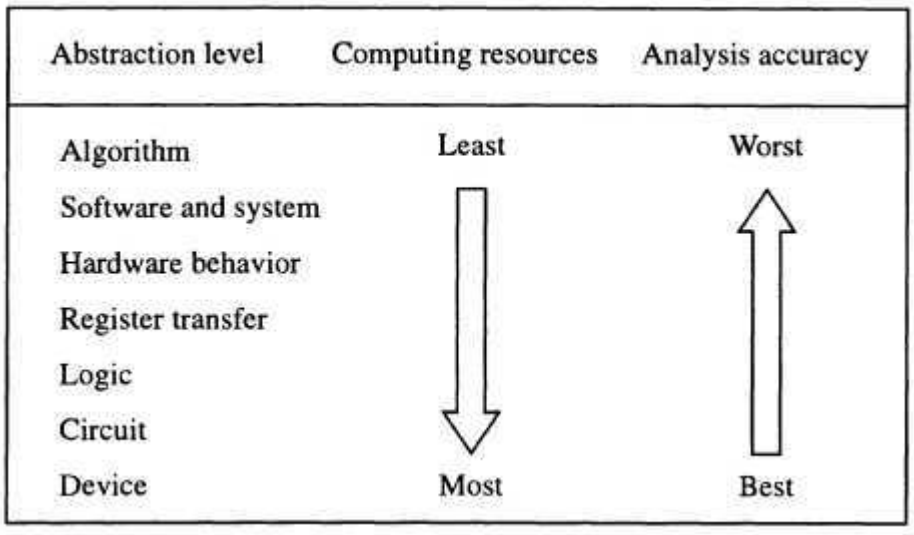
8. What is the use of simulation in VLSI design?

Computer simulation has been applied to VLSI design for several decades. Most simulation programs operate on mathematical models which mimic the physical laws and properties of the object under simulation. Today, simulation is used for functional verification, performance, cost, reliability and power analysis. Many simulation languages have been developed specifically for IC's. For example in digital logic simulation, VHDL (Very High Speed IC Hardware Description Language) and Verilog are two popular languages being used.

9. What do you know about simulation based power estimation and analysis?

Simulation-based power estimation and analysis techniques have been developed and applied to the VLSI design process . Simulation software operating at various levels of design abstraction is a key technology in the mainstream VLSI design. The main difference between simulation at different levels of design abstraction is the trade-off between computing resources (memory and CPU time) and accuracy. In general, simulation at a lower-level design abstraction offers better accuracy at the expense of increased computer resource. Circuit simulators such as SPICE attain excellent accuracy but cannot be applied to full chip analysis. Logic simulation generally can handle full-chip analysis but the accuracy is not as good and sometimes the execution speed is too slow. Behavioral-level or functional-level simulation offers rapid analysis but the accuracy is sacrificed.

10. Summarize the trade-off between computing resources and analysis accuracy at different levels of design abstraction.



11. What do you know about SPICE?

SPICE (Simulation Program with IC Emphasis) is the de facto power analysis tool at the circuit level. SPICE operates by solving a large matrix of nodal current using the Krichoff's Current Law (KCL). The basic components of SPICE are the primitive elements of circuit theory

such as resistors, capacitors, inductors, current sources and voltage sources. More complex device models such as diodes and transistors are constructed from the basic components. The device models are subsequently used to construct a circuit for simulation. SPICE offers several analysis modes but the most useful mode for digital IC power analysis is called *transient analysis.*

12. Write the advantages of SPICE power analysis.

The strongest advantage of SPICE is of cause its accuracy. SPICE is perhaps the most versatile among all power analysis tools. It can be used to estimate dynamic, static and leakage power dissipation. MOS and bipolar transistor models are typically available and it also faithfully captures many low-level phenomena such as charge sharing, cross talk and transistor body effect. In addition, it can handle common circuit components such as diodes, resistors, inductors and capacitors. Specialized circuit components can often be built using the SPICE's modeling capability.

13. Write the limitations of SPICE model.

SPICE analysis requires intensive computation resources and is thus not suitable for large circuits. Most SPICE-based simulators start to experience memory or computation limitation at several hundred to several thousand devices. Some advanced SPICE simulators can handle circuits up to ten thousand devices but simulating the entire chip is not possible. The main source of error in SPICE is seldom found in the computation process but the inherent difficulties in modeling physical components and devices.

14. Mention various types of simulation models to speed up the computation speed and memory.

(i) Tabular transistor model
(ii) Switch level analysis
(i) Gate level analysis
(ii) Architecture level analysis
(iii) Data correlation analysis in DSP systems
(iv) Monte-Carlo simulation
(v)

15. What do you know about gate level logic simulation?

Simulation-based gate-level timing analysis has been a very mature technique in today's VLSI design. The component abstraction at this level is logic gates and nets. The circuit consists of components having defined logic behavior at its inputs and outputs, such as NAND gates, latches and flip-flops. Most gate-level analysis can also handle capacitors and some can also handle resistors and restricted models of interconnect wires. Gate-level logic simulation software is one of the earliest CAD tools being developed. Today, many gate-level logic simulators are available, most of which can perform full-chip simulation up to several million gates.

16. What is dynamic power?

The dynamic power dissipated inside the logic cell is called *internal power,* which consists of short-circuit power and charging/discharging of internal nodes.

17. What is the impact of capacitance on the power analysis of CMOS circuits?

Capacitance is the most important physical attribute that affects the power dissipation of CMOS circuits. Capacitance also has a direct impact on delays and signal slopes of logic gates. Changes in gate delays may affect the switching characteristics of the circuit and influence power dissipation. Short-circuit current is affected by the input signal slopes and output capacitance loading. Thus, capacitance has a direct and indirect impact on power analysis.

18. What are the advantages of using architectural level analysis?

Architectural level analysis is also called block-level or macro-level design. The basic building blocks at this level are registers, adders, multipliers, busses, multiplexors, memories, state machines, etc. Each component performs a dedicated "high-level" function as perceived by the designer. Today, architecture-level power analysis is becoming more important because more digital circuits are now synthesized from architectural description. As VLSI chips increase in size and complexity, it has become inefficient to design each individual gate.

19. What are data correlation analysis in DSP systems?

In a digital signal processing (DSP) system, a phenomenon known as *sample correlation* has been observed. Sample correlation refers to the property that successive data samples are very close in their numerical values and consequently their binary representations have many bits in common. This is not a coincidence but a direct result of sampling a band-limited analog signal with a higher sampling rate relative to the analog signal bandwidth. Some data streams exhibit *negative correlation* (anti-correlation) in which successive samples jump from a large positive value to a large negative value. Negative correlation may occur in some digital signal coding schemes such as delta modulation. Obviously, positive or negative correlation has a significant effect on the power dissipation of a DSP system because of the switching activities on the system datapath.

20. What are the steps involved in Monte Carlo based simulation?

The estimated power dissipation P of the circuit under simulation is given by the average value of the samples, i.e.,

$$P = \frac{(p_0 + p_1 + \ldots + p_N)}{N}$$

The *sample variance*

$$S^2 = \frac{1}{N}\sum_{i=1}^{N}(p_i - P)^2$$

The number of samples required is

$$N \geq \left(\frac{t_{[N-1,\alpha/2]} S}{\varepsilon P} \right)^2$$

1. Simulate to collect one sample *Pi*

2. Evaluate sample mean *P* and variance S2

3. Check if the inequality is satisfied; if so stop, else repeat from Step 1.

This process is called *Monte Carlo power simulation.*

21. What do you know about probabilistic power analysis?

The basic model of probabilistic power analysis is very different from simulation-based approaches. A logic signal is viewed as a random zero-one process with certain statistical characteristics. We no longer know the exact event time of each logic signal switching. Instead, we only prescribe or derive several numerical statistical characteristics of the signal. The power dissipation of the circuit is then derived from the statistical quantities. The primary reason for applying probabilistic analysis is computation efficiency.

The number of statistical quantities to be analyzed is generally orders of magnitude smaller than the number of events to be processed compared to the simulation approach. Typically, only a few statistical quantities need to be computed at a given node of the circuit as opposed to thousands of events during simulation. The biggest drawback of the probabilistic approach is the loss in accuracy. Nevertheless, probabilistic power estimation technique is a crucial tool in today's digital VLSI design. The application of probabilistic power analysis techniques has mainly been developed for gate-level abstraction and above. Since probabilistic techniques are notorious for their preciseness, their applications to transistor or circuit-level networks are limited because of the high accuracy sought at this level.

PART – B

1. Explain Monte-Carlo simulation used for power estimation in logic circuits.

2. What are the steps in logic power estimation? Brief.

3. Explain the various power models used in probabilistic power estimation in any DSP system.

4. Explain the power estimation technique at the logic level..

5. Explain the probabilistic based power analysis.

UNIT V

SYNTHESIS AND SOFTWARE DESIGN

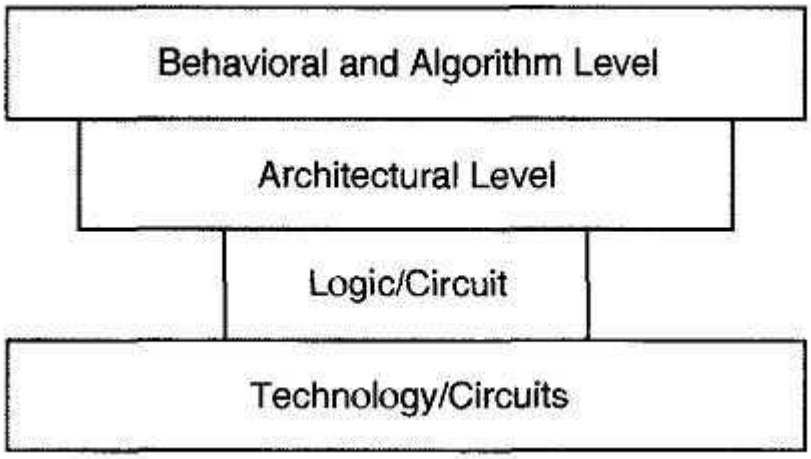
FOR LOW POWER CMOS CIRCUITS

PART – A

1. What are the behavioral level transform techniques considering DSP circuits?

Algorithm Level Transforms for Low Power
Power-Constrained Least-Squares Optimization for Adaptive and non adaptive filters
Circuit Activity Driven Architectural Transformations

2. What are possible improvements in power dissipation at various levels of design abstraction?



3. What are the two algorithm level techniques for improvement in power dissipation targeted for digital filters?

The two algorithm level techniques for improvement in power dissipation targeted for digital filters; both techniques try to reduce computation to achieve low power. The first technique uses differential coefficient representation to reduce the dynamic range of computation while the other technique optimizes the number of l's in coefficients representation to reduce the number of additions (or switching activity). Other techniques try to use multiplier-less implementations for low-power and high-performance. Since digital signal processing techniques are very well represented mathematically, algorithm level techniques can be easily applied.

4. Mention the advantages of DCM method for the low power synthesis?

The *differential coefficients method* (DCM) is an algorithm level technique for realization of low-power FIR filters with a large number of taps*(N* of the order of hundreds). The DCM relies on reducing computations to reduce power. The computation of the convolution in the canonical form for the **FIR** filter output by using the multiply-and- accumulate sequence (computing the product of each coefficient with the appropriate input data and accumulating the products), will be termed *direct-form computation.*

The algorithms for the DCM use various orders of differences between the coefficients in conjunction with stored precomputed results rather than the coefficients themselves to compute the canonical form convolution. The DCM can also lead to a reduction in the time needed for computing each convolution and thus one may obtain an added advantage of higher speed of computation.

5. State the first order difference algorithm for generating the FIR filter output.

$$\{P_k\}_{t-j} + C_k X_{j-k} \quad \text{for } k = 0, \ldots, N-2$$

The above algorithm is called the *first-order differences algorithm* for generating the **FIR** filter output. The additional storage accesses and additions incurred using this algorithm will be termed *overheads.*

6. Write the second order difference algorithm.

$$C_k X_{j-k+1} = C_{k-1} X_{j-k+1} + \delta^1_{k-2/k-1} X_{j-k+1} + \delta^2_{k-2/k} X_{j-k+1}$$

$$\text{for } k = 2, \ldots, N-1$$

7. Why Sorted Recursive Differences method is beneficial over DCM method?

One limitation of DCM is that it can be applied only to systems where the envelope generated by the coefficient sequence (and various orders of differences) is a smoothly varying continuous function; thus it was beneficial largely for low-pass **FIR** filters. But an improved version of DCM, called the *sorted recursive differences* (SRD) method, which uses recursive sorting of coefficients and various orders of differences to maximize the computational reduction. This recursive sorting is made possible by the transposed direct form of **FIR** output computation. Thus there are no restrictions on the coefficient sequence to which it is applicable (or the sequences of various orders of differences). The effective word length reduction using the DCM was not the same for each coefficient. Instead of pessimistically using the worst case reduction, one can use a simple statistical estimate for the effective reduction in the number of l's in the coefficients.

8. What is the basic idea of using the Power Constrained Least Squares(PCLS) technique for low power dissipation?

The power constrained least-squares (PCLS) technique can be applied to both nonadaptive digital filters. The basic idea in this technique is to reduce the number of l's in the representation of the coefficients such that the number of additions in a multiplier can be reduced, thus achieving low-power dissipation. However, due to changes in the coefficients representation, the performance of the filter can change. Hence, changes in the filter coefficients can be allowed within a range such that the change in performance is within the tolerance limit.

9. How the architecture-driven voltage scaling is helpful to achieve low power dissipation?

The increase in circuit delay can be possibly compensated for by scaling down the device sizes. However, in the submicrometer range the interconnect capacitances do not scale proportionately and can become dominant. Hence, it is worth looking at architectural transformations to compensate for the delay to achieve lower power dissipation by scaling down the supply voltage. One simple way to maintain throughout while reducing the supply voltage is to utilize parallel or pipe lined architecture.

10. Mention the advantage of using pipelined implementation over parallel implementation for low power design?

The method of using parallelism to reduce power has the overhead of more than twice the area and is not suitable for area constrained designs. Another approach is pipelining which has the advantage of smaller area overhead. With the additional pipeline latch, the critical path becomes maximum allowing the adder and the comparator to operate at a slower speed. If one assumes the two delays to be equal, the supply voltage can again be reduced from 5 to 2.9 V, the voltage at which the delay doubles, with no loss in throughput.

11. What are the sources of software power dissipation?

(i) The memory system can be the dominant source of power dissipation in some memory-intensive DSP applications.
(ii) System buses
(iii) Data paths in integer arithmetic logic units (ALUs) and floating-point units (FPUs)
(iii) Power overhead for control logic and clock distribution and Power management

12. List the steps involved in software power estimation.

The first step toward optimizing software for low power is to be able to estimate the power dissipation of a piece of code. This has been accomplished at two basic levels of abstraction. The lower level is to use existing gate level simulation and power estimation tools on a gate level description of an instruction processing system. A higher level approach is to estimate power based on the frequency of execution of each type of instruction or instruction sequence (i.e., the execution profile).Power estimates for each active component are then taken from a look-up table and added into the power estimate for the program.

Another approach is based on the premise that the switching activity on buses (address, instruction, and data) is representative of switching activity (and power dissipation) in the entire processor. Bus switching activity can be estimated based on the sequence of instruction op-codes and memory addresses.

The final approach we will consider is referred to as *instruction level power analysis*. This approach requires that power costs associated with individual instructions and certain instruction sequences be characterized empirically for the target processor. These costs can be applied to the instruction execution sequence of a program to obtain an overall power estimate.

13. What do you know about Instruction Level Power Analysis?

Instruction level power analysis (ILP A) defines an empirical method for characterizing the power dissipation of short instruction sequences and for using

these results to estimate the power (or energy) dissipation of a program. Three approaches have been documented for accomplishing this characterization. The most straightforward method is to directly measure the current drawn by the processor in the target system as it executes various instruction sequences. If this is not practical, another method is to first use a hardware description language model (such as Verilog or VHDL) of the processor to simulate execution of the instruction sequences. An actual processor can then be placed in an automated IC tester and exercised using test vectors obtained from the simulation. An ammeter is used to measure the current draw of the processor in the test system. A third approach is to use gate level power simulation of the processor to obtain instruction level estimates.

14. List the software power optimizations for minimum power or energy.

Software optimizations for minimum power or energy tend to fall into one or more of the following categories: selection of the least expensive instructions or instruction sequences, minimizing the frequency or cost of memory accesses, and exploiting power minimization features of hardware.

15. What are the objectives of power minimization techniques related to memory?

Power minimization techniques related to memory concentrate on one or more of the following objectives:

- Minimize the number of memory accesses required by an algorithm.
- Minimize the total memory required by an algorithm.
- Put memory accesses as close as possible to the processor.
- Choose registers first, cache next, and external RAM last.
- Make the most efficient use of the available memory bandwidth; for example, use multiple-word parallel loads instead of single-word loads as much as possible.

16. How will you minimize memory access costs by using binary search algorithm?

The binary search algorithm is not only much more efficient than linear search but also permits a fast pipelined implementation. A separate memory and processing element can be used for each level of the search tree. The encoding process can then proceed in a pipelined manner, handling eight vectors simultaneously. The clock rate can be reduced by a factor of 8 from a serial implementation. This architecture increases memory area more than twofold, but short critical paths and reduced clock permit a supply voltage reduction from 3 to 1.1 V.

Overall, memory accesses were reduced by a factor of 30 and power was scaled down by a factor of 17 compared to a system with a single serial access memory.

17. What is instruction packing?

Instruction packing permits an ALU operation and a memory data transfer to be packed into a single instruction. Much of the cost of each individual instruction is overhead that is not duplicated when operations are executed in parallel. Consequently, there can be nearly a 50% reduction in energy associated with the packing of two instructions. Similar benefits can be achieved by parallel loading

of multiple words from different banks of memory.

18. What is instruction ordering?

Instruction ordering for low power attempts to minimize the energy associated with the circuit state effect. Circuit state effect, if you recall, is the energy dissipated as a result of the processor switching from execution of one type of instruction to another. Instruction ordering then involves reordering instructions to minimize the total circuit state cost without altering program behavior.

19. List some processors that support varying levels of software control over power management.

Several processors support varying levels of software control over power management. Some examples include the Fujitsu SPARClite MB86934, Hitachi SH3, Intel486SL, and the PowerPC 603 and 604.

20. Compare the Software-based power management with Hardware-based power management.

Software-based power management has the advantage of additional information upon which to base power management decisions. Purely hardware-based power management has to make its decisions by monitoring processor activity. An incorrect decision to power down can hurt performance and power dissipation due to the cost of restoring power and system state. Processors with integrated power management provide ways to efficiently save and restore the processor state in the event of a power-down. Program execution cycles committed to power management represent a down side to software-based power management.

21. What are the levels of automated low power code generation tools?

There are two levels of tools: tools that generate code from an algorithm specification and compiler level optimizations.

22. Briefly discuss about cold scheduling algorithm.

A *cold scheduling algorithm* that is an instruction scheduling algorithm that reduces bus switching activity related to the change in state when execution moves from one instruction type to another. The algorithm is a list scheduler that prioritizes the selection of each instruction based on the power cost (bus switching activity) of placing that instruction next into the schedule. Following is the ordering of compilation phases that Su proposed in order to incorporate cold scheduling:

1. Allocate registers.
2. Pre-assemble: Calculate target addresses, index symbol table, and transform instructions to binary.
3. Schedule instructions using cold scheduling algorithm.
4. Post-assemble: Complete the assembly process.

One limitation of this approach is that it becomes difficult to schedule instructions across basic block boundaries because of the early determination of target addresses. Cold scheduling was found to obtain a 20- 30% switching activity reduction with a performance loss of 2-4%.

23. Briefly discuss about the proposed code generation and optimization methodology.

Lee et al. proposed a code generation and optimization methodology. Following is the sequence of phases that they proposed:

1. Allocate registers and select instructions.
2. Build a data flow graph (DFG) for each basic block.
3. Optimize memory bank assignments by simulated annealing.
4. Perform *as soon as possible* (ASAP) packing of instructions.
5. Perform list scheduling of instructions (similar to cold scheduling).
6. Swap instruction operands where beneficial.

The optimization phases appear to be sequenced in order from greatest to least incremental benefit. Overall energy savings on four benchmarks ranged from 26 to 73% compared to results that did not incorporate instruction packing or optimize memory bank assignments.

23. What is hardware/software co-design for low power?

Hardware/software codesign for low power is a more formal term for the problem of crafting a mixture of hardware and software that provides required functionality, minimizes power consumption, and satisfies objectives that could include latency, throughput, and area.

24. What do you know about reconfigurable computing?

"Reconfigurable computing" is a growing area of research in processor design that could motivate radical new requirements for software design tools. **It** also presents new opportunities and challenges for low-power systems design. In reconfigurable processors, some portion of the interconnect and logic can be modified at run time. This should allow the processor to be closely optimized to each of a wide variety of applications. Reconfiguration can be implemented at any of several levels of granularity, ranging from the gate level up to architectural level changes. The reconfigurable components are commonly implemented using field programmable gate arrays.

25. What are the categories on the impact of processor design decisions on opportunities for power minimization in software?

The design decisions are organized into three categories: memory system design, processor architecture, and power management.

26. What are the key points to be considered in making software design decisions consistent with the objective of power minimization?

Key objectives to be considered are the following:

- Choose the best algorithm for the problem at hand and make sure it fits well with the computational hardware. Failure to do this can lead to costs far exceeding the benefit of more localized power optimizations.
- Minimize memory size and expensive memory accesses through algorithm

transformations, efficient mapping of data into memory, and optimal use of memory bandwidth, registers, and cache.

- Optimize the performance of the application, making maximum use of available parallelism.
- Take advantage of hardware support for power management.
- Finally, select instructions, sequence them, and order operations in a way that minimizes switching in the CPU and data path.

PART – B

1. Explain low power techniques and the trade offs involved in synthesis process.
2. Explain how power optimization can be incorporated in software design.
3. Explain the steps involved in synthesis for low power.
4. Explain in detail the software design for low power.