QUESTION BANK

Name of the Department : **Electronics and Communication Engineering**

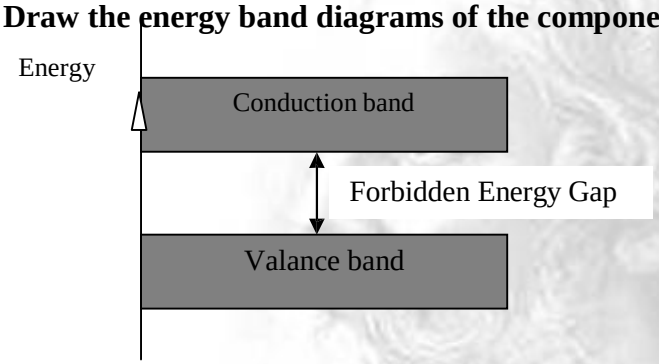
Subject Code & Name : **VL4152 & Digital CMOS VLSI Design**

Year & Semester : **I & I**

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER

PART-A

1. Draw the energy band diagrams of the components that make up the MOS system.



2. What is body effect Coefficient?

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Where, γ = body effect Coefficient.

3. Determine whether an nMOS transistor with a threshold voltage of 0.7 V is operating in the saturation region if V_{GS}=2 V and V_{Ds}=3 V.

$V_{DS} > V_{GS} - V_t$
3 V > 2 V – 0.7 V
3 V > 1.3 V
Therefore, the nMOS transistor is operating in the saturation region.

4. Write down the equation for describing the channel length modulation effect in nMOS transistor.

Because of channel length modulation effect in the saturation region of a nMOS transistor,

$$I_{ds} = \beta \frac{(Vgs - Vds)^2}{2}(1 + \lambda V_{ds})$$

Where,

β= a constant
V_{gs}= gate to source voltage
V_{ds} = drain to source voltage
λ = channel length modulation factor

5. Brief the different operating regions of MOS system.

Non-saturated region: IR drop in the channel is same throughout the channel and can take as average value as $V_{DS}/2$.The effective gate voltage V_g is given by, $V_g = V_{GS} - V_t$ .Where, V_t is threshold voltage needed to invert the change under the gate and to establish the channel.

$$I_{DS} = C_0 \mu \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V^2_{DS}}{2}\right]$$

Saturation region: The device enters into saturation when $V_{DS} = V_{GS} - V_t$, because at this point the IR drop in the channel equals the effective gate to channel voltage. The current through the channel remains fairly constant for any further increase in V_{DS} .

$$I_{DS} = C_0 \mu \frac{W}{2L}(V_{GS} - V_T)^2$$

6. Why the tunneling current is higher for nMOS transistor than pMOS transistor with silica gate?

Tunneling current is higher for nMOS transistor than pMOS transistor with SiO_2 gate dielectrics because the electrons tunnel from the conduction band while the holes tunnel from the valance band.

7. What is the objective of layout rules?

The main objective of layout rules is to build reliable functional circuits with small area. The rules represent a compromise between performance and yield. The rules also represent tolerance that ensures very high probability of correct fabrication and subsequent operation.

8. What are the factors that cause drain punch through in MOS transistor?

- Higher voltage to gate causing breakdown
- Arcing across the thin oxide

9. What are the drawbacks of NMOS inverters compared with CMOS inverters?

The most important advantage of CMOS is the very low static power consumption in compare with NMOS technology. On the other hand, CMOS technology is more complex to fabricate then NMOS technology, so it is more expensive. However, almost every today digital circuits are CMOS. We want to use NMOS only when we want to fabricate fast and low-cost a simple circuit.

10. List the various issues in technology-CAD.

- Design Rule Checking
- Circuit Extraction

11. What is meant by Epitaxy?

This involves growing a single-crystal film on the silicon surface by subjecting the silicon wafer surface to an elevated temperature and a source of dopant material.

12. What are the special features of twin tub process?

- Allow optimization of n-type and p-type transistor
- Doping can be controlled easily
- Latch-up is achieved

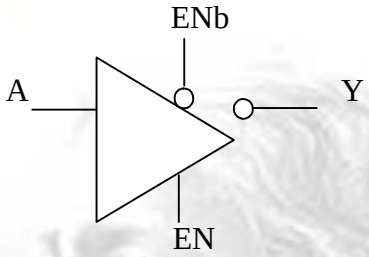
13. Define noise margin.

Noise margin is related to DC voltage characteristics. This allows determining the allowable noise voltage on the input of a gate so that the output will not be corrupted.

14. Draw the symbol for tristate inverter and brief about its operation.

When EN= 0 and ENb= 1, output Y of the inverter is in tristate.

When EN= 1 and ENb= 0, output Y of the inverter is the complement of input A.



14. Compare nMOS and pMOS devices.

nMOS	pMOS
Electrons are the majority carriers. When positive voltage is applied on gate, number of electrons will increase. So, conductivity of channel is increased.	Majority carriers are holes.

15. Compare enhancement and depletion mode devices.

S.NO.	Enhancement mode	Depletion mode
1	FET has no channel with zero gate-to-source voltage.	Device has a conducting channel with zero gate bias and will not turnoff until sufficient reverse bias is applied to its gate.
2	Have separate gate bias voltage (or) have its gate connected to its drain to use it as active load.	The gate is connected with the source to use it as load.

16. What are the non-ideal I-V effects?

- Velocity Saturation and Mobility Degradation
- Channel Length Modulation
- Body Effect
- Sub-Threshold Condition
- Junction Leakage
- Tunnelling
- Temperature Dependence
- Geometry Dependence

17. What are the different MOS layers?

- Diffusion layer
- Polysilicon layer
- Metal layer

18. What are four generations of Integration Circuits?

- SSI (Small Scale Integration)
- MSI (Medium Scale Integration)
- LSI (Large Scale Integration)
- VLSI (Very Large Scale Integration)

19. Give the advantages of IC.

- Size is less
- High Speed
- Less Power Dissipation

20. Give the variety of Integrated Circuits.

- More Specialized Circuits
- Application Specific Integrated Circuits(ASICs)
- Systems-On-Chips

21. Define Short Channel devices.

Transistors with Channel length less than 3- 5 microns are termed as Short channel devices. The ratio between the lateral & vertical dimensions is reduced in this channel.

22. Define Threshold voltage.

The threshold voltage V_t for a MOS transistor can be defined as the voltage between the gate and the source terminals below which the drain to source current effectively drops to zero.

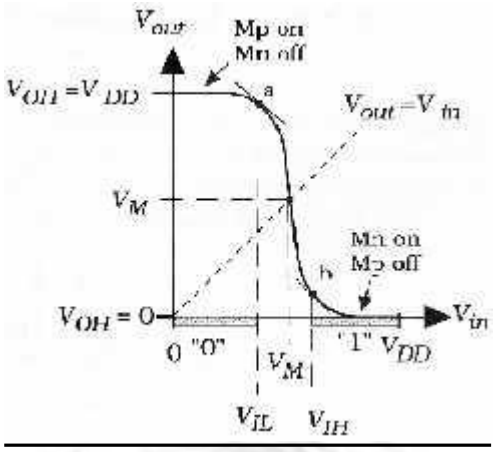
23. Define body effect or substrate bias effect.

The threshold voltage V_t is not a constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This effect is called the body effect or substrate bias effect.

24. What are the secondary effects of MOS transistor?

- Threshold voltage variations
- Source to drain resistance
- Variation in I-V characteristics
- Subthreshold conduction
- CMOS latchup

25.Plot the D.C transfer characteristics of a CMOS inverter.



PART-B

1. (i) Explain the DC transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation
   (ii) Discuss the principles of constant field and lateral scaling. Write the effects of the above scaling methods on the device characteristics.
2. (i) Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics.
   (ii) Describe in detail about body effect and its effect in MOS device.
3. Explain the operation of following MOS transistor
   (i) NMOS enhancement.
   (ii) PMOS enhancement.
4. Illustrate the following electrical properties of MOS device:
   (i) Threshold voltage.
   (ii) Small signal AC characteristics.
5. Discuss about following MOS capacitance model
   (i) Simple MOS capacitance model
   (ii) Detailed MOS gate capacitance model.
   (iii) MOS device capacitance.
   (iv) Detailed MOS diffusion capacitance model.
6. Explain about MOS resistance model with neat diagram.
7. Explain in detail about second order effects of MOS transistor.
8. (i) Briefly discuss about the Non ideal I-V characteristics of MOS transistor.
   (ii) Describe the important properties used for the estimation of resistance in MOS resistance model.

UNIT II COMBINATIONAL LOGIC CIRCUITS

PART-A

1. What is the influence of voltage scaling on power and delay?

Voltage scaling on delay is expressed by a factor of 1/S and that of power is unity.

2. Express T_{PHL} and T_{PLH} in terms of C_{load}.

T_{PHL} is the propagation delay in seconds for the transfer of high to low and T_{PLH} is the propagation delay in seconds for the transfer of low to high.

3. Write the expressions for the logical effort and parasitic delay of n input NOR gate.

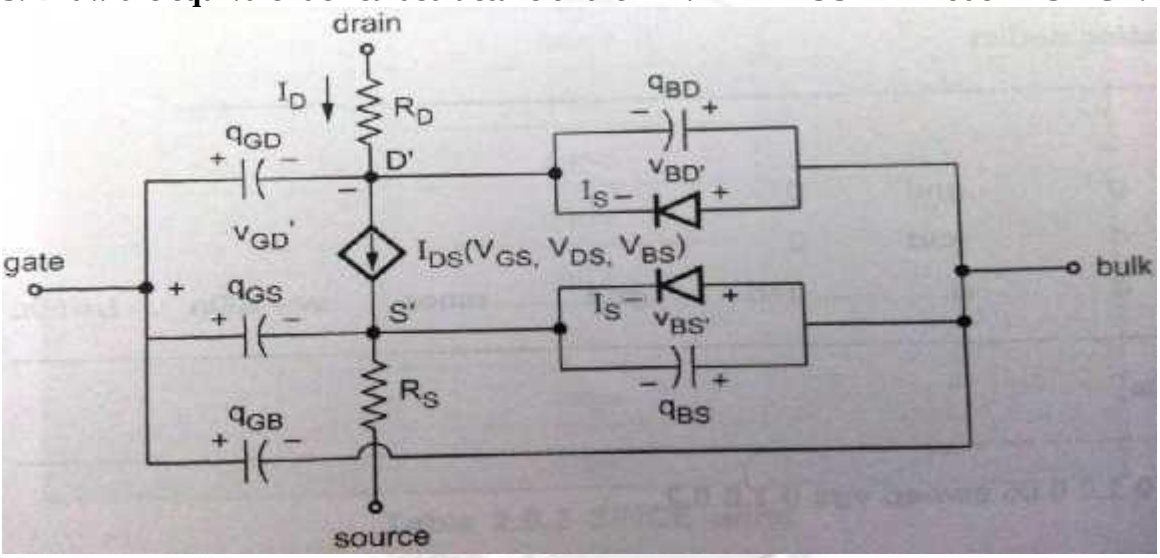
Logical effort of n input NOR	Parasitic delay of n input NOR
(2n + 1)/3	N

4. Why does interconnect increase the circuit delay?

Interconnect increases the circuit delay for the following two reasons:

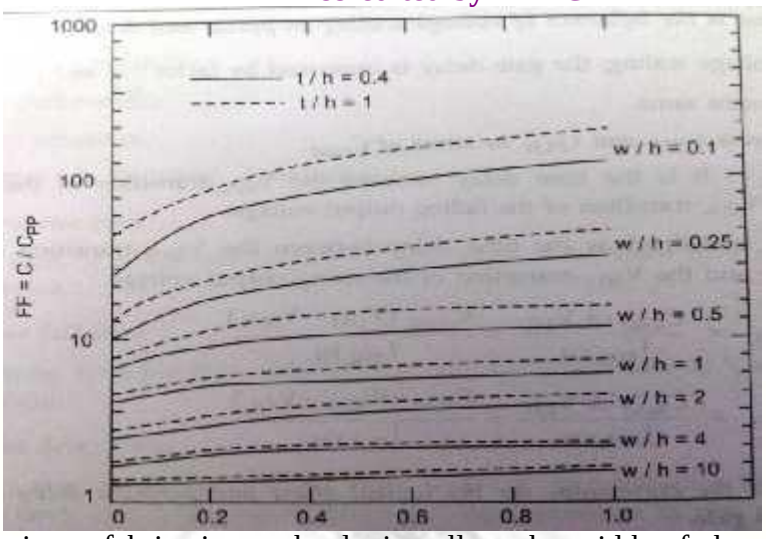
- Wire capacitance adds loading to each gate.
- Long wires with significant resistance contribute distributed RC delay or flight time.

5. Draw the equivalent circuit structure of the LEVEL 1 MOSFET model in SPICE.



6. Brief about the variation of the fringing field factor with the interconnect geometry.

Fig. Shows the variation of the fringing-field factor FF= C_{total}/C_{pp}, as a function of (t/h), (w/h) and (w/l). It can be seen that the influence of fringing fields increases with the decreasing (w/h) ratio, and that the fringing-field capacitance can be as much as 10-20 times larger than the parallel-plate capacitance.



The sub-micron fabrication technologies allow the width of the metal lines to be decreased somewhat, yet the thickness of the line must be preserved in order to ensure structural integrity. This situation, which involves narrow metal lines with a considerable vertical thickness, is especially vulnerable to fringing field effects.

7. Give the effect of supply voltage and temperature variations on the CMOS system performance.

Supply voltage varies due to various factors such as tolerances of voltage regulator, IR drops along supply rails, and di/dt noise. If the supply voltage is specified at ± 10% around nominal at every logic gate then the variation has a uniform distribution with a half-range of 10% of V_{DD}, so tolerance of supply voltage leads to ± 10% delay variations. Power supply variations also appear in noise budgets.

Drain current decreases with the increase in temperature. The junction temperature of a transistor is the sum of the ambient temperature and the temperature rise caused by power dissipation in the package. The temperature rise is determined by the power consumption and package thermal resistance.

8. What are the factors that cause static power dissipation in CMOS circuits?

The static power dissipation is caused by,

- Total leakage current (I_{static})
- Supply voltage (V_{DD})

9. What is meant by design margin?

The circuit behavior is determined by process variation, supply voltage and operating temperature. The circuit should be design to reliable operate over all extremes of these three variables. The variations can be modelled with Gaussian or uniform statistical distributions.

10. How do you define the term "device modeling"

The functional relationship among the terminal electrical variables of the device that is to be modeled is called device modeling.

11. List the various power losses in CMOS circuits.

- Static power dissipation – Due to the leakage current drawn from the power supply

- Dynamic power dissipation – Due to switching transient current and charging and discharging of load capacitance.

12. Define rise time and fall time.

- Rise time, τ_r is the time taken for a waveform to rise from 10% to 90% of its steady-state value.
- Fall time, τ_f is the time taken for a waveform to fall from 90% to 10% of its steady-state value.

13. What is pull- down device?

A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

14. Write an expression for power dissipation in CMOS inverter.

$P_{total} = P_s + P_d + P_{short}$

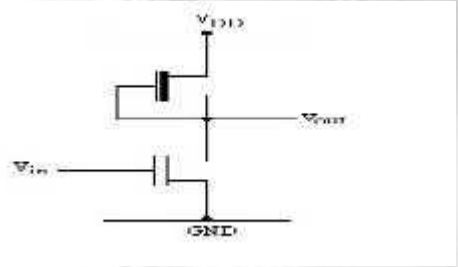
Where,

P_s = static power dissipation

P_d = dynamic power dissipation

P_{short} = short-circuit power dissipation

15. Draw the circuit of an MOS inverter.



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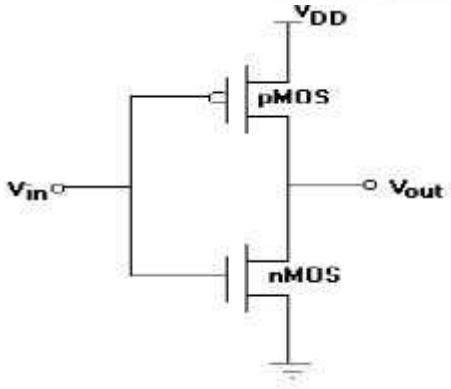
16. Draw the circuit of a CMOS inverter.



17. What are the advantages of CMOS inverter over the other inverter configurations?

- The steady state power dissipation of the CMOS inverter circuit is negligible.
- The voltage transfer characteristic (VTC) exhibits a full output voltage wing between 0V and VDD. This results in high noise margin.

18. What is pull-up device?

A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

19. How do you prevent latch up problem?

Latch-up can be reduced by reducing the gain of parasitic transistor and resistor. Latch-up is prevented in two ways.

- Latch-up resistant CMOS process
- Layout technique

20. Define the lambda layout rules.

Lambda-based design rules are based on the assumption that one can scale a design to the appropriate size before manufacture. The assumption is that all manufacturing dimensions scale equally, an assumption that "works" only over some modest span of time.

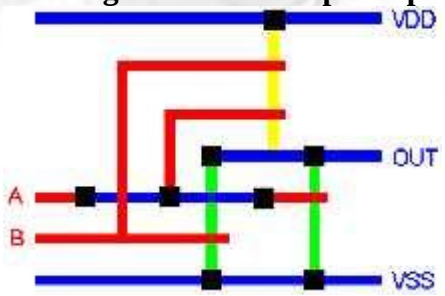
21. Discuss any two layout design rules.

- Lambda design rules – specify the layout constraints in terms of a single parameter and allow linear, proportional sealing of all geometrical constraints.
- Micron rules – specify the layout constraints such as minimum feature sizes and minimum allowable feature separation are stated in terms of micrometer dimension.

22. What is stick diagram?

Stick diagram is the symbolic diagram drawn in different colors to show the various layers used in fabrication and their relative positions.It does not show the spacing between layers. Stick diagrams convey layer information through color codes or monochrome encoding. It acts as an interface between symbolic circuit and the actual layout.

23. Draw the stick diagram of a static gate with an output expression Y = (A+B)'.



24.Mention the method of design rules.

- Process specific CMOS rules
- Scalable CMOS rules

25. Define. 'SCMOS design rule.'

It is the scalable CMOS design rule in which the MOS elements are designed by a scalable unit λ. By simply changing the value of λ for different CMOS technology, the designs can be altered easily.

26. Define. 'Power dissipation'. Mention its types.

It is the power consumed by the circuit elements and usually it is dissipated as heat. There are two types of power dissipation.

- Static power dissipation
- Dynamic power dissipation
-

27. What is static power dissipation?

It is the power dissipated when the device is off and it is due to leakage current through the devices.

28. How do you define dynamic power dissipation?

It is the power dissipated during the switching current and charging and discharging of load capacitances.

PART-B

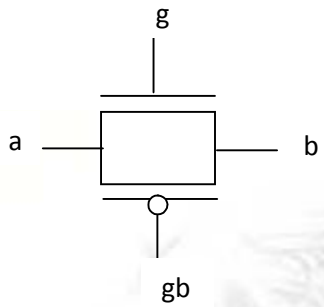
1. (i) Realize the function Y = (A + B + C).D using CMOS compound gate. Draw the stick diagram and layout diagram.
   (ii) Develop the necessary stick diagram and layout for inverter, NAND and NOR gates.
2. Discuss about the lambda based design rules for NMOS and CMOS transistors.
3. Draw the circuit layout and stick diagram for
   (i) Two input XOR gate.
   (ii) CMOS inverter.
4. Describe about layout design rules in detail with necessary diagrams.
5. (a) Realize the following function using CMOS
   (i) F (A, B, C) = A'BC + AB'C + ABC'
   (ii) Y= (A+B) (C+D)
   (b) Explain about delay estimation, logical effort and transistor sizing with example.
6. (i) Draw the static CMOS logic circuit for the following expression.
   (a) Y = A . B . C . D
   (b) Y = D (A + BC) (8)
   (ii) Discuss in detail about the characteristics of CMOS transmission gate.
7. What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS?
8. With neat sketch, illustrate the operation of pass transistor DC characteristics.
9. Write short notes on
   (i) RC delay models.
   (ii) Elmore delay model.
   (iii) Linear delay model.
   (iv) Logical effort delay model.
10. (i) Explain the operation, important properties, advantages and limitations of static CMOS design.
    (ii) Explain about the problem of charge sharing and the methods to overcome it.
11. (i) Describe the static CMOS design using basic gates and compound gates.
    (ii) List the various applications of transmission gate.

UNIT III SEQUENTIAL LOGIC CIRCUITS

PART-A

1. Write a note on CMOS transmission gate logic.

Transmission gate consists of an nMOS transistor in parallel with gates controlled by complementary signals 'g' and 'gb' as shown in figure.



2. What are the advantages of differential flip flops?

- Accept inputs and produce outputs in true and complementary form,
- Circuits are built from clocked sense amplifiers to respond with small differential input voltages.

3. State the reasons for the speed advantage of CVSL family.

CVSL has a potential speed advantage because all the logics are performed using nMOS transistors. This will reduce the input capacitance.

4. Mention the qualities of an ideal sequencing method.

An ideal sequencing method has the following qualities,

- Introduce no sequencing overhead
- Allow sequencing elements back-to-back with no logic in between
- Grant the designer flexibility in balancing the amount of logic in each clock cycle
- Tolerate moderate amounts of clock skew without degrading performance
- Consume zero area and power

5. What is meant by transmission gate?

Transmission gate provides good conduction path between X and Y. It is constructed by connecting nMOS and pMOS parallel.

6. What are synchronizers?

Synchronizers accept an input that can change at arbitrary times and produces an output aligned to the synchronizers clock. This has a nonzero probability of producing an metastable output.

7. State any two criteria for low-power logic design.

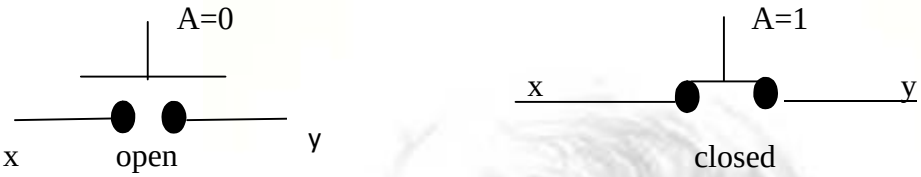
Choose a suitable process

- Channel width capacitance per micron is 2 fF/μm
- Process is run at lower V_{DD}
- Static power increases with advanced process

8. What is CBIC?

A cell based ASIC uses pre-designed logic cells are known as standard cells or CBIC.

9. Draw an assert high switch condition if input = 0 and input = 1.



10. What is meant by ratioed logic?

In ratioed logic, a gate consists of an nMOS pull-down network that realizes the logic function and a simple load device, which replace the entire pull-up network. A ratioed logic which uses a grounded pMOS load is referred to as a pseudo-nMOS gate.

11. What is true single phase clocked register?

The True single-phase clocked register (TSPCR) uses a single clock, CLK. For the positive latch, when CLK is high, the latch is in the transparent mode and corresponds to two cascaded inverters; the latch is non-inverting, and propagates the input to the output. On the other hand, when CLK=0, both inverters are disabled, and the latch is in the hold mode.

12.Write short notes on Latch up.

Latch up is the generation of a low-impedance path in CMOS chips between the power supply and the ground rails due to interaction of parasitic PNP and NPN bipolar transistors. These BJTs forms a silicon-controlled rectifier with positive feedback and virtually short circuit the power and the ground rail.This causes excessive current flows and potential permanent damage to the devices.

13. Name the techniques used to prevent Latch up.

- By reducing the BJT gains by lowering the minority carrier lifetime through Gold doping of the substrate.
- By using p+ guardband rings connected to ground around nMOS transistors and n+ guard rings connected to VDD around pMOS transistors to reduce Rw and Rsub and to capture injected minority carriers before they reach the base of the parasitic BJT.
- By placing substrate and well contacts as close as possible to the source connections of the MOS transistors to reduce the values of Rw and Rsub.
- By using Bi-CMOS circuits

14. Define Pipelining

Pipelining is a popular design technique often used to accelerate the operation of the data path in digital processors.The major advantages of pipelinig are to reduce glitching in complex logic networks and getting lower energy due to operand isolation.

PART-B

1. Explain the Bi-stability principle associated with static latches and registers.
2. Elaborate on the differences between latches and registers with necessary timing diagrams.
3. Explain the operation of Static SR flip flops built using NOR and NAND gates.
4. What is the common approach for constructing an edge triggered register? Explain the operation of a register based on master-slave configuration.
5. Explain the timing metrics for sequential circuits with neat diagrams.
6. Illustrate the impact of clock skew and jitter on the performance of a sequential system.
7. Illustrate the basic concept of clock synthesis and synchronization using Phase –Locked loop.
8. Discuss in detail various pipelining approaches to optimize sequential circuits.
9. Explain the methodology of sequential circuit design of latches and flip-flops.
10. Describe about pulse and sense amplifier based registers.
11 Write short notes on Nonbistable sequential circuits..

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES

PART-A

1. Write a note on partition and MUX technique.

Multiplexers and demultiplexers are used to improve the observability in testing. Transmission gate multiplexers occupy less space with increased speed. Circuit partitioning and multiplexers increases the chip area and circuit delay.

2. Differentiate the PLA from the PAL.

PLA	PAL
Programmable Logic Array	Programmable Array Logic
Programmable AND gates followed by programmable OR gates	Programmable AND gates followed by fixed OR gates
Programming is difficult than PAL	Easy to program than PLA
More flexible	Less flexible
High cost	Low cost
Large size	Small size

3. Give the application of PLA.

- I/O applications
- Control logic applications
- Used in data path logic

4. Mention the drawback of ripple carry adder.

The ripple carry adder has increased time delay since the output of any full adder in not valid until the incoming carry bit is valid. So the adder performs always slower.

5. Explain the terms generate and propagate in CLA adders.

The addition of two 1-digit inputs A and B is said to generate if the addition will always carry, regardless of whether there is an input carry (equivalently, regardless of whether any less significant digits in the sum carry).

The addition of two 1-digit inputs A and B is said to propagate if the addition will carry whenever there is an input carry (equivalently, when the next less significant digit in the sum carries).

6.Write the merits and demerits of carry select adders.

The speed of these adders is high since the upper and lower words are summed simultaneously. But these adders costly and occupies more area.

7.Define. 'Multiplier'.

Multiplier do the binary multiplication which is similar to the result of logical AND operation.

8 .Define. 'Cross talk'.

When an interconnect line is placed in close to any other interconnect line, there is parasitic capacitance realized between them. So any of the changes in one line will induce stray signal on other lines. This phenomenon is called as cross talk.

PART-B

1. Describe ripple carry adder and derive the worst case delay with example.
2. Describe the concept of monolithic and logarithmic look ahead adder.
3. Design a 16 bit carry bypass and carry select adder and discuss their features.
4. Explain the methods to accumulate partial products in array form.
5. Illustrate the partial product generation logic associated with a multiplier.
6. Discuss the data paths in digital processor architectures.
7. Design the arithmetic logic unit (ALU) of 64 bit high end microprocessor and arithmetic operators involved in design.
8. Define shifter and give short notes on (i) Barrel shifter (ii) Carry save multiplier
9. Explain the concept of a high speed adder.
10. Discuss on memory architectures and memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES

PART-A

1. Give the expression of inductance for a cylindrical wire.

The inductance of a cylindrical wire above a ground plane is given by,

$$Inductance L = \frac{\mu}{2\pi} \times ln\left(\frac{4h}{d}\right)$$

Where, μ = permeability of the wire
d = diameter of the wire

h = height above the ground plane

The inductance of a cylindrical wire on a chip is given by,

$$Inductance L = \frac{\mu}{2\pi} \times ln\left(\frac{8h}{w} + \frac{w}{4h}\right)$$

Where,

w= width of the conductor h = height above the substrate

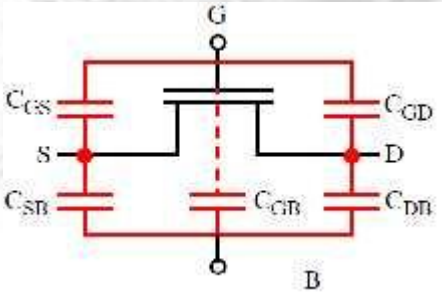
2. Why the parasitic components present in MOS devices should be estimated?

The parasitic components present in MOS devices will reduce the speed of operation since the parasitic capacitance will take considerable time to charge and discharge due to the presence of parasitic resistance. So these components have to be estimated and eliminated.

3. What are the various capacitances realized in MOS device?

- Gate capacitances
  - ❖ Gate to Source capacitance (C_{GS})
  - ❖ Gate to Drain capacitance (C_{GD})
  - ❖ Gate to Bulk capacitance(C_{GB})
- Diffusion capacitance
  - ❖ Source to Bulk capacitance (C_{SB})
  - ❖ Drain to Bulk capacitance (C_{DB})
- Routing capacitance

4. Draw the diagram showing MOS capacitances.



5. What is routing capacitance?

It is the capacitance realized between metal and poly layers and usually modeled like parallel plate capacitor.

6. Obtain the relation between rise time and fall time.

$$fall Time\ tf = \frac{4C}{\beta n.Vdd}$$

And, βn = 2 βp

So,

$$fall Time\ tf = \frac{4C}{2\beta p.Vdd}$$

But, $Rise\ Time\ tr = \frac{4C}{\beta p.Vdd}$

$$fall\,Time\ tf = \frac{tr}{2}$$

7. Derive the delay time in terms of rise time and fall time.

$$Delay\ Time\ due\ to\ rise\ rime\ tdr = \frac{tr}{2}$$

$$Delay\ Time\ due\ to\ fall\ rime\ tdf = \frac{tf}{2}$$

$$Average\ Delay\ Time\ td = \frac{tdr+tdf}{2} = \frac{\frac{tr}{2}+\frac{tf}{2}}{2} = \frac{tr+tf}{4}$$

8. Define 'Transistor Sizing'.

The process of determining the size of nMOS and pMOS transistor for a optimum driving circuit is called as Transistor sizing.

9. What is transport delay model?

Transport delay model represents the propagation delay of signals from the module inputs to its outputs in Verilog.

10. Write a note on transport delay.

The transport delay model is defined using the reserved word transport. This delay is used to model transit delays. The transport delay removes the requirement that inputs persist at least for the delay time. The signal will assume its new value after specified delay.

11. Enumerate the features of synchronizers.

- A single flip-flop can be introduced between the asynchronous input and synchronous system. This flip-flop ensures the synchronization between the two and will improve the MTBT.
- Adding second flip-flop reduce the chance of output going metastable stack. The output from first-flop may go valid, before the second flop is clocked.
- Adding get another flop will reduce the probability that its output will be unstable even more.

12. Give the comparison between structural and switch level modeling.

- Structural modeling describes a digital logic networks in terms of the components that make up the system.
- Verilog allows switch-level modeling that is based on the behavior of MOSFETs. Digital circuits at the MOS-transistor level are described using the MOSFET switches.

PART-B

1. Explain in detail about interconnect parameters.
2. Write short notes on electrical wire models.
3. Discuss on timing classification of digital systems.
4. Explain briefly about synchronous design.
5. Describe about self-timed circuit design.