QUESTION BANK

Name of the Department : Electronics and Communication Engineering. M.E VLSI Design

Subject Code & Name : AP4152 & Advanced Digital System Design

Year & Semester : I & I

UNIT-I

SEQUENTIAL CIRCUIT DESIGN

PART-A

1. **Distinguish between synchronous and asynchronous sequential circuits.** (NOV/DEC 2009)

Synchronous sequential circuit	Asynchronous sequential circuit
Memory elements are clocked flip flops	Memory elements are either unclocked flip flops or time delay elements
The change in input signals can affect memory element upon activation of clock signal	Change in input signals can affect memory element at any instant of time
The maximum operating speed of clock depends on time delays involved	Because of absence of clock, asynchronous circuits can operate faster than synchronous circuits
Easier to design	More difficult to design

2. **What is meant by edge triggering?Give the difference between the edge triggering and level triggering.** (APR/MAY 2010,MAY/JUNE 2012,NOV/DEC 2010)

   The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

   Level triggering canges state either at positive level or at negative level.

3. **State the differences between Mealy and Moore state machines.** (APR/MAY 2011)

Mealy state machine	Moore state machine
Its output is a function of present state only	Its output is afunction of present state as well

	as present input
Input changes does not affect the output	Input changes may affect the output of the circuit
It requires more number of states for implementing same function	It requires less number of states for implementing same function.

4. **How do you eliminate the race around condition in a JK flip-flop?** (NOV/DEC 2010)

To avoid the race around condition an edge trigggered or pulse triggered JK flip flop is created. In this flip-flop, the output changes only at positive edge or anegative edge of the clock.

5. **Define skew and clock skew.**

The phase shift between the rectangular clock waveforms is referred to as skew and the time delay between the two clock pulses is called clock skew.

6. **Compare the ASM chart with a conventional flow chart.** (NOV/DEC 2009, MAY 2013)

ASM chart	Conventional chart
It describes the sequence of events as well as the timing relationship between the states of a sequential controller and the events that occur while going from one state to the next.	It describes the procedural steps and decision paths of an algorithm in a sequential manner without taking into consideration their time relationshiop.

7. **What are the basic building blocks of a algorithmic state machine chart?** (APR/MAY 2011)

State box, decision box and conditional box

8. **What is state table?** (MAY/JUNE 2012)

A tabular representation of the state changes that occur in a sequential circuit.For the design of sequential counters we have to relate present states and next states. The table which represents the relationship between present states and next states, is called state table.

9. **What is synchronous sequential circuit?** (NOV 2013)

A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.

10. **What is a clocked sequential circuit?**

Synchronous sequential circuit that use clock pulses in the inputs of memory elements are called clocked sequential circuit. One advantage as that they don't cause instability problems.

11. What is an iterative circuit?

The simplest form of an iterative circuit consists of a linear array of combinational cells with signals between cells traveling in only one direction. parallel adder is an example of an iterative circuit that has four identical cells.

12. Define state assignment.

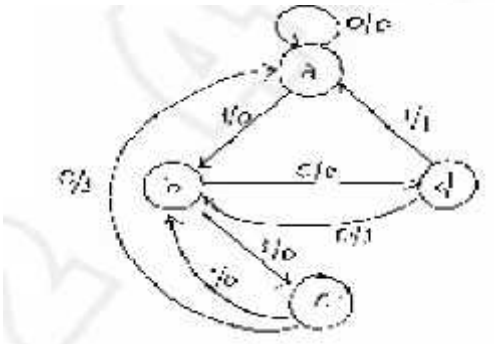
The state assignment is one step in the design of sequential circuits which assigns binary values to the states in such a way that it reduces the cost of the circuit hat drives the flip-flops.

13. Why is state reduction necessary?

The state reduction is a technique that reduces the number of states in the sequential circuit by keeping only one state for two or more redundant/equivalent states. This reduces the number of required flip-flops and logic gates, reducing the cost of the final circuit. Two states are said to be redundant or equivalent, if every possible set of inputs generate exactly same output and same next state.

PART-B

1. Explain how the behavior of clocked synchronous sequential network is described by a state table and discuss a method of state table reduction example.
2. Explain the relation between state diagrams and ASM charts.
3. Design a clocked sequential machine using T flip-flops for the following state diagram (use straight binary assignment.



4. Describe the modeling of clocked synchronous sequential network.
5. Design a parallel unsigned binary multiplier using ASM chart.
6. Perform an analysis of clocked synchronous mealey machine with a D-flip flop with an assumed example.
7. Design a sequence detector to detect the sequence 11010 using D flipflops.

8. Design an iterative circuit for even parity generator.

9. Explain the three main components of ASM chart with an example.

UNIT- II

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

PART-A

1. What is an asynchronous sequential circuit?

The sequential circuits in which the change in input signals can affect memory elements at any instant of time are called asynchronous sequential circuits.

2. Distinguish synchronous and asynchronous sequential circuits? (NOV/DEC 2010)

Synchronous sequential circuit	**Asynchronous sequential circuit**
Memory elements are clocked flip flops	Memory elements are either unclocked flip flops or time delay elements
The change in input signals can affect memory element upon activation of clock signal	Change in input signals can affect memory element at any instant of time
The maximum operating speed of clock depends on time delays involved	Because of absence of clock, asynchronous circuits can operate faster than synchronous circuits
Easier to design	More difficult to design

3. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.

Fundamental mode	Pulse mode
Circuit designs assume that the inputs to the synchronous circuit will change when the circuit is stable.	The requirement limiting input changes to only one variable also applied to pulse mode circuits.
Do not permit the input state changes until the circuit has reached a total stable state	The width of the input pulse are critical to circuit operation, circuitry must be added to ensure the input variables are pulses whose widths fall within the required boundaries.

Primitive flow table is derived from state table	Primitive flow table is derived from timing diagram

4. What are Hazards? Give its types (NOV/DEC 2009,2010,NOV 2013, MAY 2013)

Several types of timing problems exist in the logic circuit due to propagation delay path. These timing problems are called hazards. Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays.

Two types of hazards: Static hazard and Dynamic hazard.

5. What is static hazard?

A static hazard exists if a signal is supposed to remain at particular logic value when an input variable changes its value, but instead the signal undergoes a momentary change in its required value.

6. What is dynamic hazard?

The hazard in which output changes three or more times when it should change from 1 to 0 or from 0 to 1 is called dynamic hazard.

7. What are static 0 and static 1 hazards?

In a logic circuit, if output goes momentarily 0 when it should remain a 1, the hazard is known as static-1 hazard. On the other hand, if the output goes momentarily 1 when it should remain a 0, the hazard is known as static-0 hazard.

8. What is the cause of essential hazard?

An essential hazard is caused by unequal delays along two or more paths that originate from the same input. Such hazards are eliminated by adjusting the amount of delays in the affected path.

9. What are hazard free digital circuits?

If a combinational circuit is implemented using SOP formula with no product terms containing a variable and its complement and in which additional terms are included to avoid static 1 hazard , then such a network is free of static 0 hazards as well as dynamic hazards.

If a combinational circuit is implemented using POS formula with no product terms containing a variable and its complement and in which additional terms are included to avoid static 0 hazard , then such a network is free of static 1 hazards as well as dynamic hazards.

Combinational circuits free of static and dynamic hazards are called as hazard free digital circuits.

10. What are the two types of asynchronous sequential circuits? (APR/MAY 2011)

Pulse mode and fundamental mode asynchronous sequential circuits.

11. Give the comparison between state assignment synchronous circuit and state assignment asynchronous circuit.

In synchronous circuit, the state assignments are made with the objective of circuit reduction. In asynchronous circuits, the objective of state assignment is to avoid critical races.

12. Define flow table in asynchronous sequential circuit.

In asynchronous sequential circuit state table is known as flow table because of the behaviour of the asynchronous sequential circuit. The stage changes occur in independent of a clock, based on the logic propagation delay, and cause the states to flow from one to another.

13. Write short note on shared row state assignment.

Races can be avoided by making a proper binary assignment to the state variables.Here, the state variables are assigned with binary numbers in such a way that only one state variable can change at any one state variable can change at any one time when a state transition occurs. To accomplish this, it is necessary that states between which transitions occur be given adjacent assignments. Two binary are said to be adjacent if they differ in only one variable.

14. Explain the procedure for state minimization.

1. Partition the states into subsets such that all states in the same subsets are 1 equivalent.
2. Partition the states into subsets such that all states in the same subsets are 2 equivalent.
3. Partition the states into subsets such that all states in the same subsets are 3 equivalent.

15. What are races?

When two or more binary state variables change their value in response to a change in an input variable, a race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

16. Define critical race.

If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.

17. What is data synchronizer?

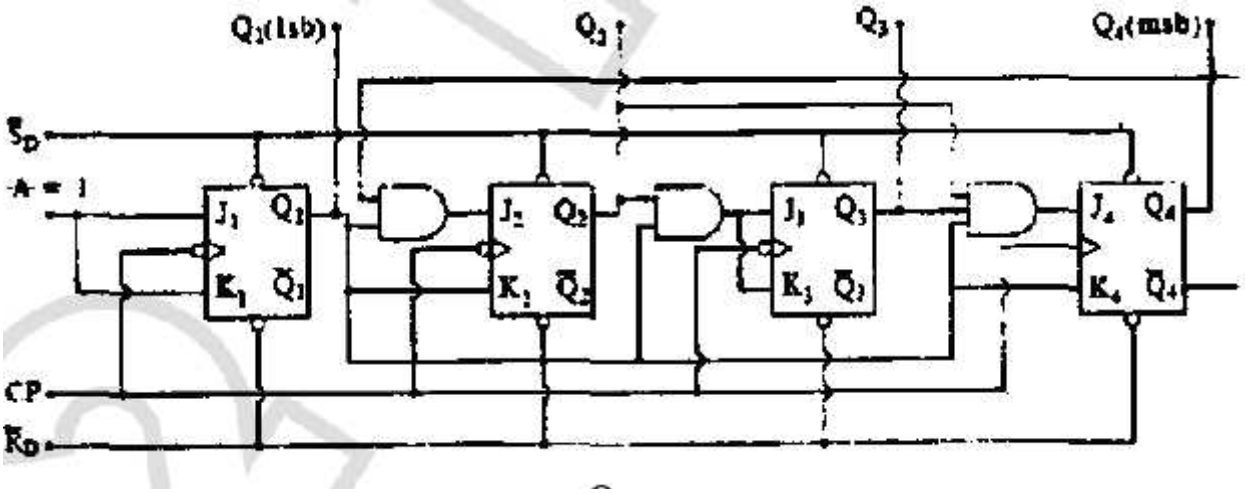
Data synchronizer is a circuit that synchronizes a system where several modules are using their own clocks but no common system clock is available. It takes all asynchronous inputs and synchronize them.

18. What is the purpose of mixed operating mode asynchronous circuits?

A mixed operating mode or self-synchronization is used to solve the critical races and hazards due to unequal propagation delay paths in asynchronous sequential circuits.

PART-B

1. Write short notes on races and hazards that occur in asynchronous circuits. Discuss a method used for race free assignment with example.
2. What are called as essential hazards? How does the hazard occur in sequential circuits? How can the same be eliminated using SR latches? Give an example.
3. What is an hazard? What are the types of hazards? Check whether the following circuit contains an hazard or not $Y=x_1x_2+x'_2x_3$. If the hazard is present, demonstrate its removal.
4. For the circuit shown in figure, write down the state table and draw the state diagram and analyze the operation.

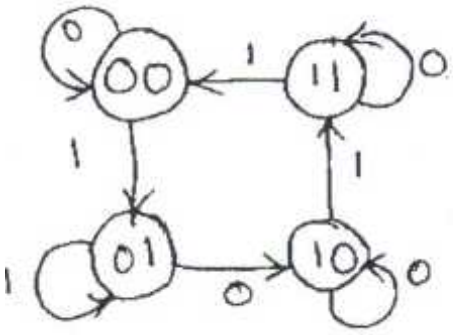


5. Writ short notes on

   i) Incompletely specified state machines

   ii) Hazard free switching circuits.

6. Determine static-1 hazard static-0 hazards for the following function and obtain the hazard free circuit $z=x_1x_2+x_2y$.
7. Obtain a primitive flow table , a minimal row flow table and transition table for a fundamental mode asynchronous sequential network meeting the following requirement.
   i) There are 2 inputs x1 and x2 and a single output z
   ii) The inputs never change simultaneously.
   iii) The output is always to be 0 when $x_1=0$, independent of the value of x_2
   iv) The output is to become 1 if x_2 changes while $x_1=1$ and is to remain 1 until x_1 becomes 0 again.
8. i) Write short notes on shared row state assignment with an example.
   ii) A sequential circuit has three D flip flops. A,B and C and one input x.It is desired by the following flip flop input functions.
   $D_A=(BC'+B'C)x+(BC+B'C')x'$
   $D_B=A$ and $D_C=B$
   Derive the state table for the circuit and draw two state diagrams for x=0 and other for x=1.
9. Explain the design of Vending Machine Controller.
10. For the state diagram shown in fig. design asynchronous sequential circuit using JK flip flop(16)



11. i) Differentiate critical races from non critical races.
    ii) Explain the steps involved in the reduction of state table.
12. Design a hazard-free asynchronous circuit that changes state whenever the input goes from logic 1 to logic 0.
13. Discuss in detail the analysis and design of asynchronous sequential circuit with suitable examples.

14. Discuss about Data synchronizers.
15. Explain the mixed operating mode asynchronous circuits.

UNIT- III

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

PART-A

1. What do you know about fault diagnosis?

In a circuit, the task of determining whether a fault is present or not is called fault detection and the task of isolating the fault is called fault location. The combined task of fault detection and location is called as fault diagnosis.

2. What is a test vector and a test set?

An input combination in which the presence of a fault produces an output different from the fault-free output is known as a test vector (TV).

The set of vectors used for testing the circuit is called the test set.

3. What is test generation?

Test generation is the process of finding the set of test vectors that can detect faults in a circuit.

4. What are the types of logical faults?

Stuck-at, bridging and crosspoint faults are three important types of logical faults.

5. What is stuck-at fault?

A stuck-at fault is said to have occurred if a signal line appears to have to have its value fixed at either a logical 1 or a logical 0, irrespective of the input signals applied to the circuit. When the signal line is always a logical 1(0), the fault is known as a stuck-at-one fault or SA1(stck-at-0 or SA0) fault.

6. What is a bridging fault?

A bridging fault is said to have occurred if two signals lines or shorted together. It may be either an AND- or an OR- type of bridging fault.

7. What are crosspoint faults?

Faults that occur in programmable logic arrays due to extra or missing devices 9 such as diode or transistor) are called crosspoint faults.

8. What is an essential test vector(ETV)?

If a fault is detected by one and only one test vector is an essential test vector(ETV).

9. What are the disadvantages of fault table method?

Fault table method is infeasible for larger circuits due to excessive time complexity and memory storage requirements.

10. State the principle behind path sensitization method.

The main idea behind the path sensitization method is to create a sensitized path in order to move the effect of the fault at any line in the circuit to primary output. Suppose that it is required to detect a SA0 fault on a line. Then it is essential that a test vector create a change on that line and ensure that the change can be seen at a primary output. In other words, the test vector must produce a 1 on that line, and the path from the line to the output must be sensitized so that the output clearly shows whether the signal on the line under consideration is 0 or 1. Then the fault can be detected. This is the principle of path sensitization method.

11. What are the three important steps for test generation using path sensitization approach?

- A path is found from test line g to the output.
- The input signals necessary to produce the appropriate signal at g(opposite the fault value) are determined.
- The path from g to the output is sensitized and other inputs are determined by back propagation.

12. What is the drawback of path sensitization method?

The single path sensitization method works well only for fanout free circuit and it can fail in circuits with reconvergent fanout.

14. What is the purpose of using Boolean difference method?

The Boolean difference method is an algebraic technique for the test generation in which the test vectors are generated by utilizing the properties of Boolean algebra.

15. What is D-algorithm? What are the advantages of D-algorithm over Boolean difference method?

The D-algorithm is the first algorithmic method for generating tests for non-redundant combinational circuits.

The D-algorithm generates a test for every fault in a circuit, if such a test exists. It uses less computation time and less memory space, and hence it is more efficient than Boolean difference method. It can also identify redundant faults by proving that no corresponding test exists.

16. What is fault tolerance? What are the fault tolerant techniques present in logic circuits?

Fault tolerance can be defined as the ability of the circuit to function correctly despite the presence of faults.

Two types: i) Static redundancy techniques ii) Dynamic redundancy techniques.

17. What is the purpose of compact algorithm?

The compact algorithm derives a Foldable Compatibility Matrix(FCM) that gives all the information required to fold a given PLA.

18. What are the faults that can occur in PLA?

The crosspoint fault model is the most popular fault in PLA. Two types of crosspoint faults can occur: The extra crosspoint fault and the missing crosspopint fault. They produce four different types of faults based on their effect on the functions realized by the PLA.

- Growth (G) faults
- Shrinkage (S) faults
- Appearance (A) faults
- Disappearance (D) faults

19. What are the major goals of DFT(Design For Testability)?

- Tests should remain valid in the presence of undetectable faults
- Compact test sets should also be computationally simple to derive
- The design procedure to achieve testability must not add undue complexity to the logic design process
- The extra hardware needed to enhance testability must be low
- The speed of operation must not deteriorate
- It must be possible to apply the tests and evaluate the response using simple hardware, so as to provide built-in self-test capability, if possible
- The test set derived must have very high coverage of all multiple faults

20. What are the advantages of BIST(Built-In-Self-Test) over external testing?

- Access to internal points of a chip is limited because internal points can be controlled only through the external I/O pins of the chip.
- The speed at which test vectors can be applied to the circuit under test is limited by the characteristics of the external tester. Often, testing at the maximum operating speed of the chip is not possible, and some timing-dependent faults may elude detection.

  BIST techniques are aimed at overcoming the problems and limitations of external testing.

PART-B

1. Explain various ways of testing sequential circuit and explain any one in detail.
2. Discuss the following: (i) Path sensitization
   (ii) Fault tolerant techniques
3. Explain the test generation and masking cycle in PLA.
4. Discuss about the design for testable (DFT) schemes.
5. Explain fault table method with an example.
6. Discuss about various testability algorithm employed in digital system design.
7. Discuss in detail about BIST.

UNIT- IV

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

PART-A

1. What is PLD?

   PLD or Programmable Logic Device is a general name for a digital integrated circuit capable of being programmed to provide a variety of different logic functions.

2. **List basic types of programmable logic devices.**

   1. Programmable Read Only Memory (PROM)
   2. Programmable Logic Array (PLA)
   3. Programmable Array Logic (PAL)

3. **Mention few applications of PLA and PAL.**

   Sequential circuits and combinational circuits

4. **What is PAL? How does it differ from PLA?**

   It is a programmable logic device with a fixed OR array and a programmable AND array.

PLA	PAL
Both AND and OR arrays are programmable	OR array is fixed and AND array is programmable
Costliest and complex than PAL	Cheaper and simpler
AND array can be programmed to get desired minterms	AND array can be programmed to get desired minterms

5. **Mention the steps in the design process of programmable logic devices.**

   - Specification of the function that the desired circuit should perform
   - Generation of Boolean equations required to implement the function
   - Minimization of the Boolean equations
   - Generation of a fuse map from the Boolean equations
   - Logic simulation
   - Programming the selected device
   - Testing

6. **What is GAL?**

The Generic Array Logic introduced by Lattice Semiconductor Company contains a programmable AND array, a fixed OR array, and an output stage. GAL devices are EEPLDs, which means that they can be reprogrammed while still in the circuit board.

7. **How the finite state machine can be realized using PLD languages?**

In PLD languages, state machines are programmed with a procedural language like regular software. The PLD has its own syntax and restrictions that permit it to work with the models of the actual devices it is to program.

8. **What are FPGAs?**

Field Programmable Gate Array(FPGA) is an IC that contains an array of identical logic cells with programmable interconnections. The user can program the functions realized by each logic cell and the connections between the cells. The FPGAs consist of an array of logic cells or Configurable Logic Blocks(CLBs).

9. **What are the basic types of FPGASs?**

Three basic types are: antifuse, EPROM and SRAM based FPGAs.

10. **What are the features of Xilinx FPGA?**

- Xilinx uses a high-density, high speed CMOS process to implement its FPGA.
- Three modules are : CLBs, I/O blocks and switching matrices for interconnections.
- The CLB consists of a combinational logic array, data multiplexers and flip-flops.
- The combinational array function is performed by a 32x1 look-up table that realizes any five-variable Boolean function.
- The program controlled multiplexers are used to route data internally in the CLB.

11. **What are the basic elements present in the architecture of Xilinx XC4000 series?**

The basic architecture of XC4000 consists of an array of configurable logic blocks (CLBs), a variety of local and global routing sources, IOBs, programmable I/O buffers, and a SRAM based configuration memory.

PART-B

1. With a neat sketch, give a technical insight on programmable array logic devices and mention their application.
2. Give a detailed account on performing synchronous design using programmable devices(any one type).
3. Explain the realization of state machines using PLD.
4. Describe the Xilinx FPGA architecture.
5. Explain the architecture and application of FPGA.
6. With neat diagrams, explain the Xilinx 4000 series architecture with I/O blocks.

UNIT- V

SYSTEM DESIGN USING VERILOG HDL

PART-A

1. What is Verilog HDL?

Verilog HDL is a hardware description language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate-level to the switch-level.

2. Mention the important features of Verilog HDL.

- Verilog HDL has a syntax that describes precisely the legal constructs that can be used in the language.
- It uses about 100 keywords pre-defined, lowercase, identifiers that define the language constructs.
- Any comment begins with two slashes(//) and multiple comments can be written in between /*….comments….*/.
- Blank spaces are ignored and names are case sensitive.

3. What are the major design steps for modeling in Verilog HDL?

- Design entry
- Simulation
- Synthesis and timing verification
- Fault simulation

4. What are the various kind of operators in Verilog HDL?

- Boolean logical
- Unary reduction logical
- Bitwise logical
- Relational
- Binary arithmetic
- Unary arithmetic

5. What are the various kind of data types in Verilog HDL?

Primary data types are for modeling registers (reg) and nets (wire). Other data types are:

Value set, Vectors, Integer, real and time register, arrays, memories, parameters and strings.

6. What are the modeling techniques used for describing a module?

- Gate level modeling / Structural modeling
- Data flow modeling
- Behavioral modeling

7. Compare structural and behavioral modeling.

In structural design, Verilog uses components or gates to model the system.

It is sometimes possible to directly describe the behavior or functionality of a circuit. Such a modeling style is called behavioral modeling which is very similar in syntax and semantics to that of a high level programming language. A behavioral description models the system as to how the outputs behave with the inputs.

8. What is meant by logic synthesis?

Logic synthesis is the process of converting a high-level description of the design into an optimized gate-level representation, giving a standard cell library and certain design constraints.

9. What is the process in compilation and simulation of verilog code?

A portion of verilog might be suitable for one environment but not for another. The designer does not wish to create two versions of verilog design for the two environments. Instead, the designer can specify that the particular portion of the code be compiled only if a certain flag is set. This is called conditional compilation.

A designer might also want to execute certain parts of the verilog design only when the flag is set at run time. This is called conditional execution.

10. What is the purpose of using Test bench?

A test bench has three main purposes:

- To generate stimulus for simulation
- To apply this stimulus to the module under test and collect output responses
- To compare output responses with expected values.

11. Write the verilog code for the up/down counter using behavioral description.

```
module UpDownCounter (Control, ClockB, Counter);
  input Control, ClockB;
  output [1:0] Counter;
  reg [1:0] Counter;

  always @ (negedge ClockB)
    if (Control)
      Counter <= Counter + 1;
    else
      Counter <= Counter - 1;
endmodule
```

12. Write the verilog code for the 2-bit comparator using behavioral description.

```
module Comparator (A, B, EQ, GT, LT, NE, GE, LE);
  parameter NUMBITS = 2;
  input [NUMBITS:1] A, B;
  output EQ, GT, LT, NE, GE, LE;

  reg [5:0] ResultBus;
  // Bit 5 is EQ, bit 4 is GT, 3 is LT, 2 is NE,
  // 1 is GE and 0 is LE.

  always @ (A or B)
    if (A == B)
      ResultBus = 6'b100011;
    else if (A < B)
      ResultBus = 6'b001101;
    else // (A > B)
      ResultBus = 6'b010110;

  assign {EQ, GT, LT, NE, GE, LE} = ResultBus;
endmodule
```

13. Write the verilog code for the simple multiplexer.

```
module SimpleMultiplexer (DataIn, SelectAddr, MuxOut);
  input [0:3] DataIn;
  input [0:1] SelectAddr;
  output MuxOut;

  assign MuxOut = DataIn[SelectAddr];

  endmodule
```

14. Write the verilog code for the full adder.

```
// Define a 1-bit full adder
module fulladd(sum, c_out, a, b, c_in);

// I/O port declarations
output sum, c_out;
input a, b, c_in;

// Internal nets
wire s1, c1, c2;

// Instantiate logic gate primitives
xor (s1, a, b);
and (c1, a, b);

xor (sum, s1, c_in);
and (c2, s1, c_in);

or  (c_out, c2, c1);

endmodule
```

PART-B

1. Explain logic system, operators and data types for modeling in verilog HDL.
2. Write the verilog code based on Behavioral description for the following: (i) Serial adder
   (ii) Up/Down counter
3. Explain about synthesis for finite state machines.
4. Write the verilog code for combinational and sequential circuits(any one example).
5. Write the verilog code for shift register.
6. Write the verilog code for the design of simple microprocessor.